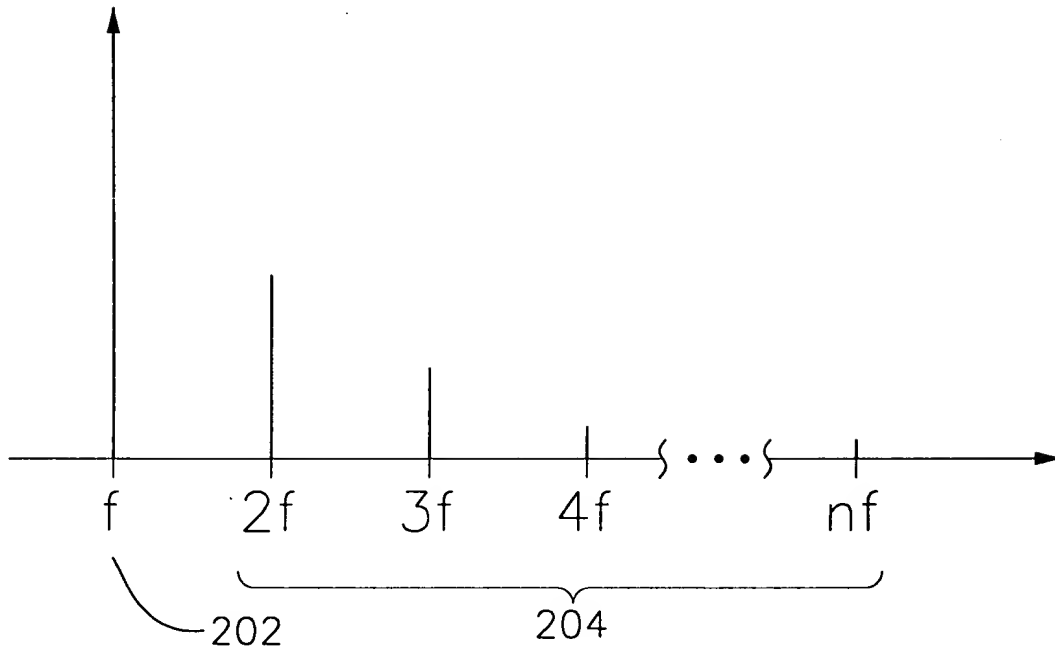


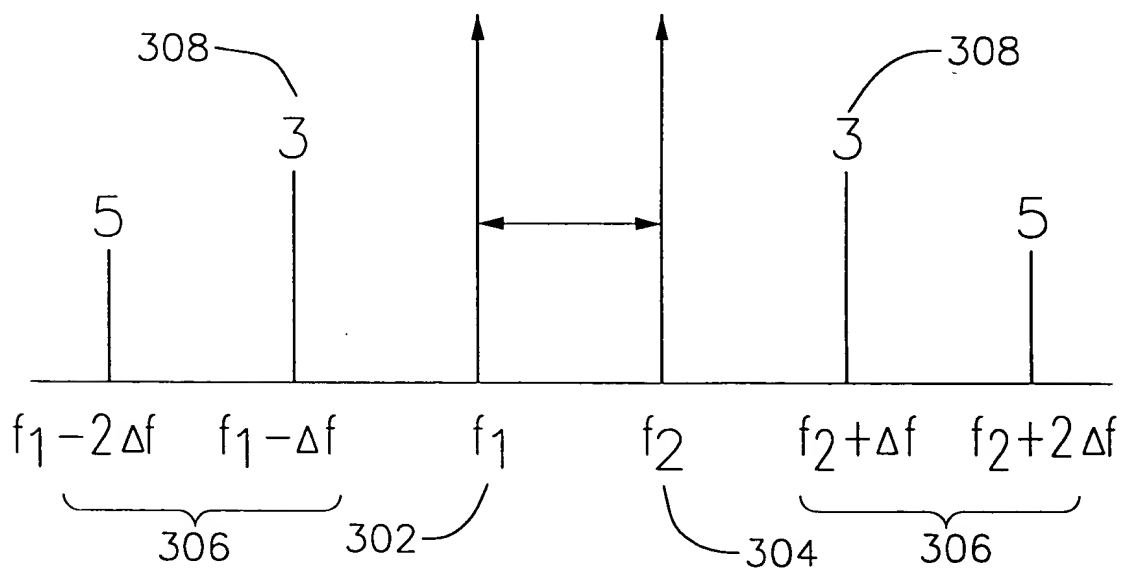




*FIG. 2*

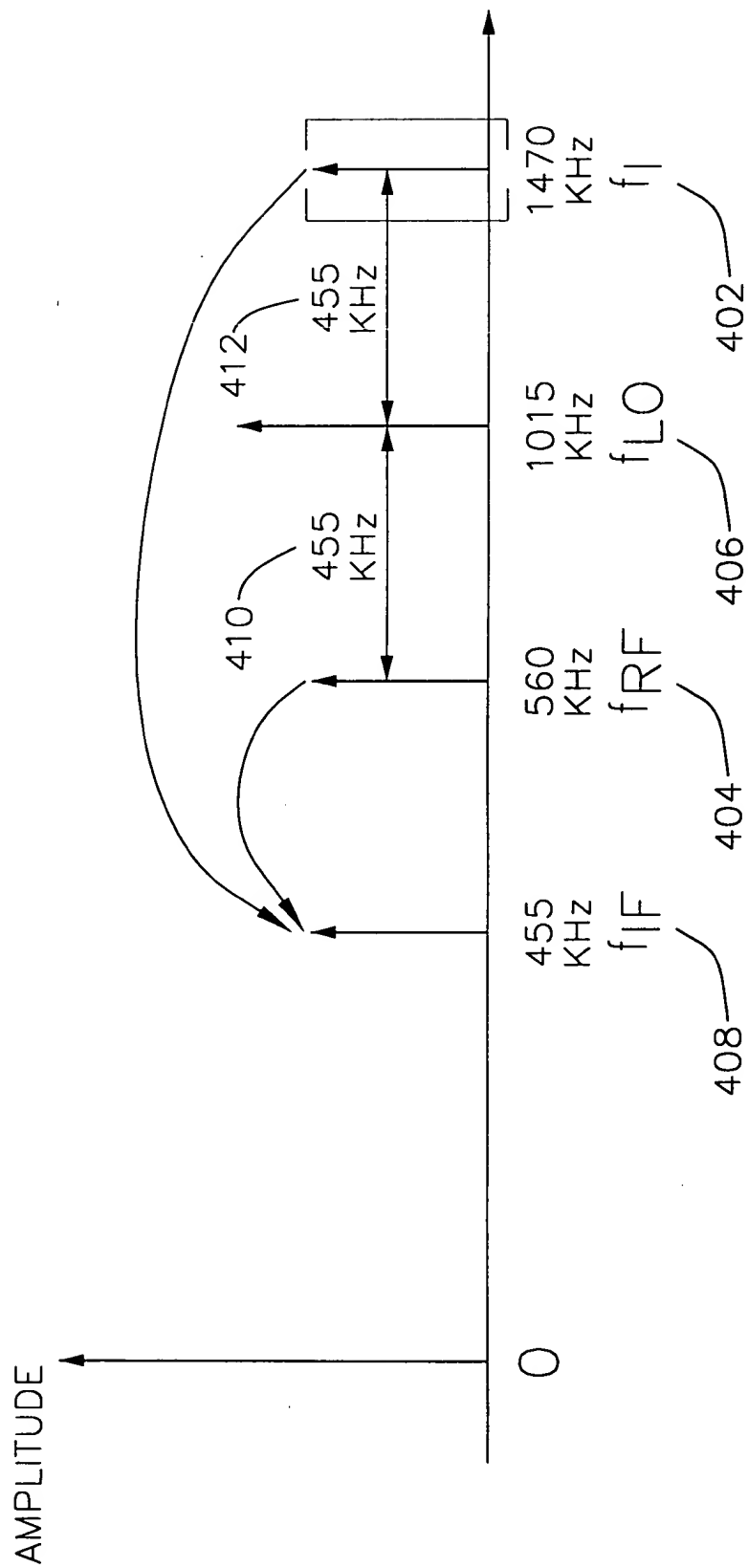


*FIG. 3*  
PRIOR ART



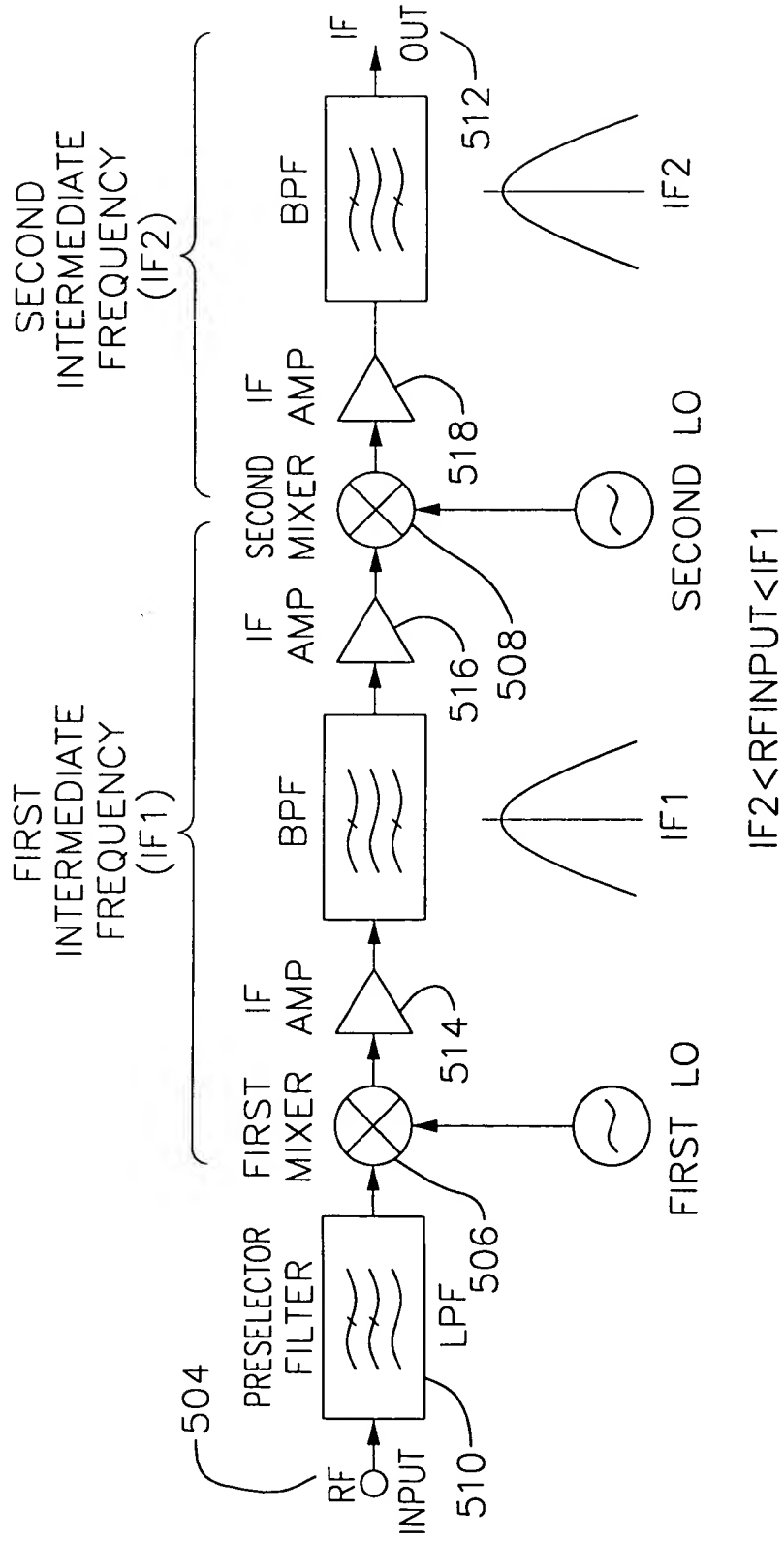
PRIOR ART

PRIOR ART



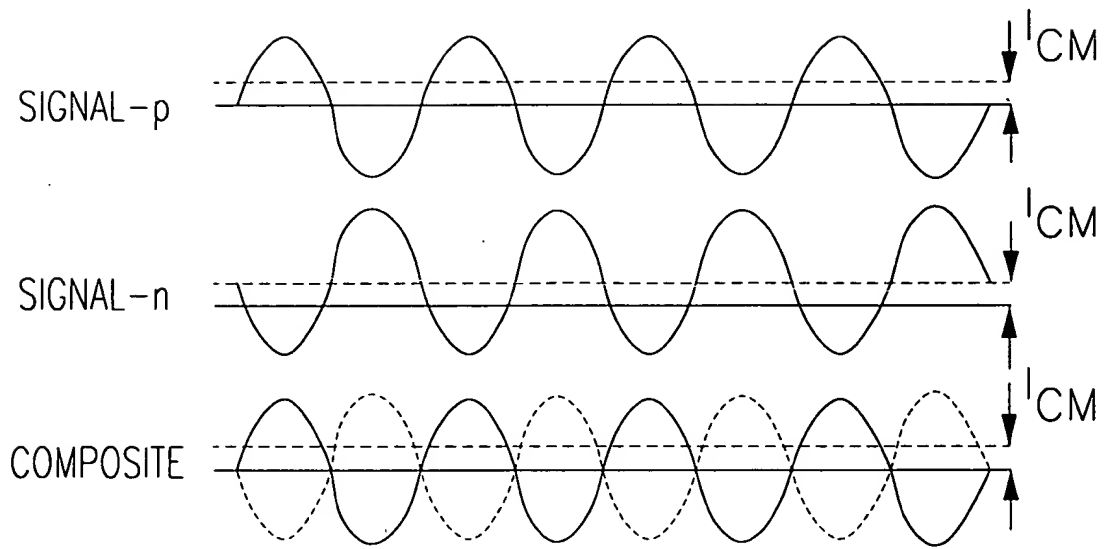
**FIG. 5**

DUAL CONVERSION RECEIVER

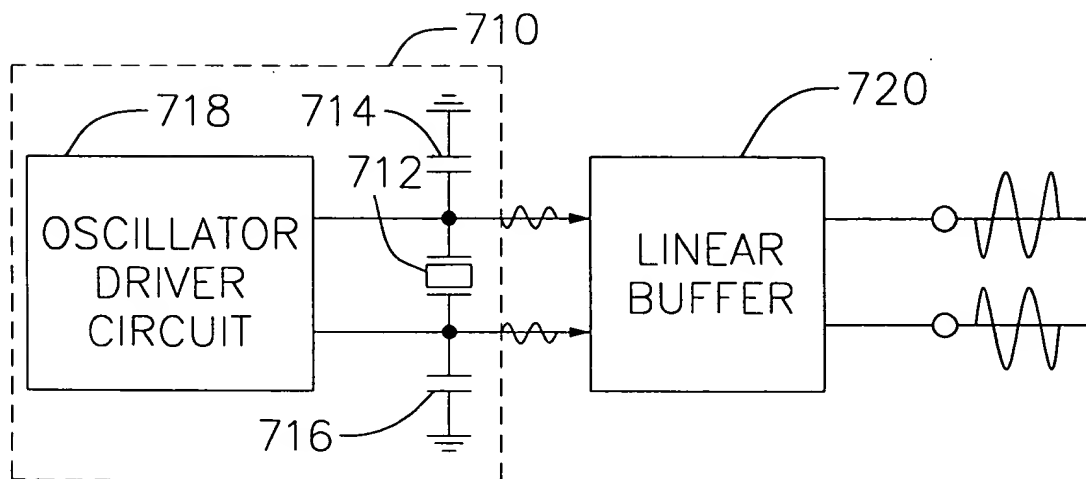




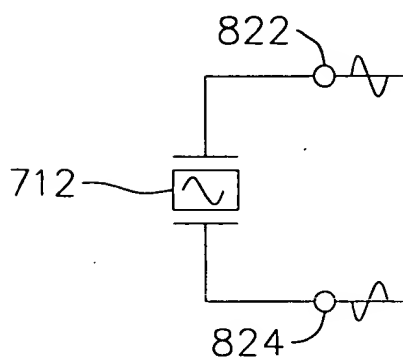
*FIG. 6*



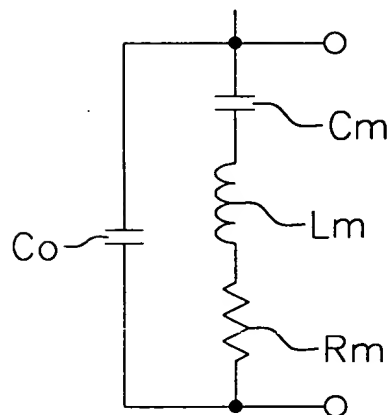
*FIG. 7*



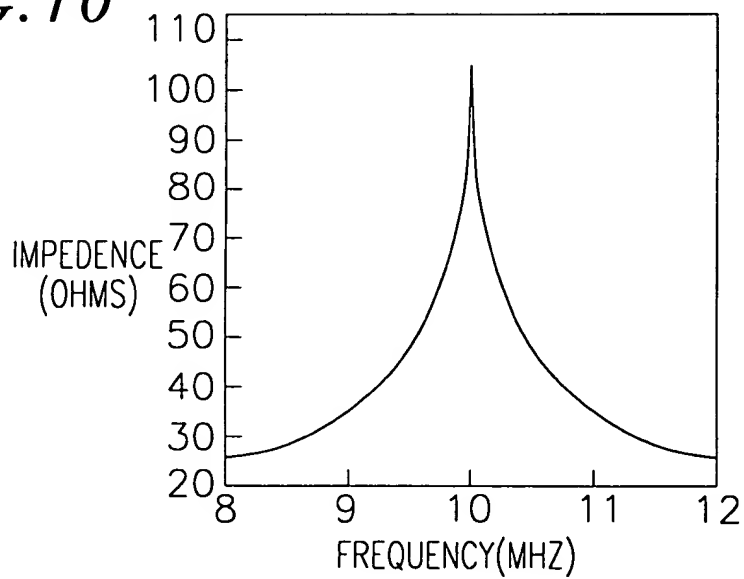
*FIG. 8*



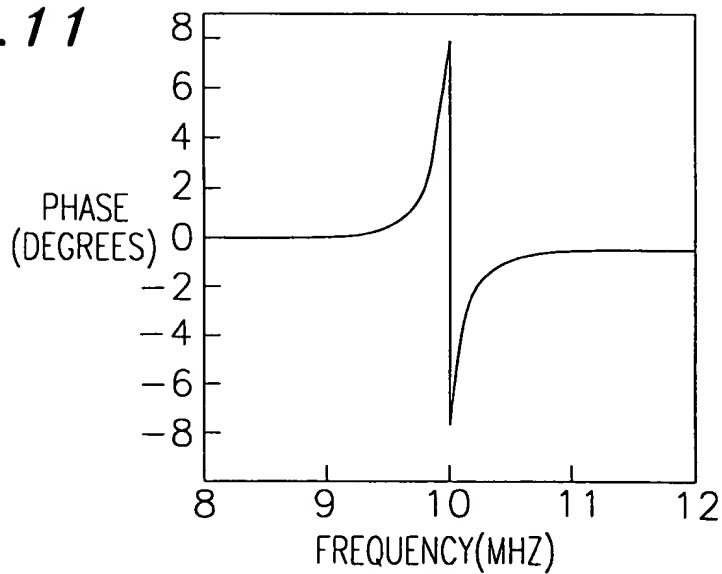
*FIG. 9*



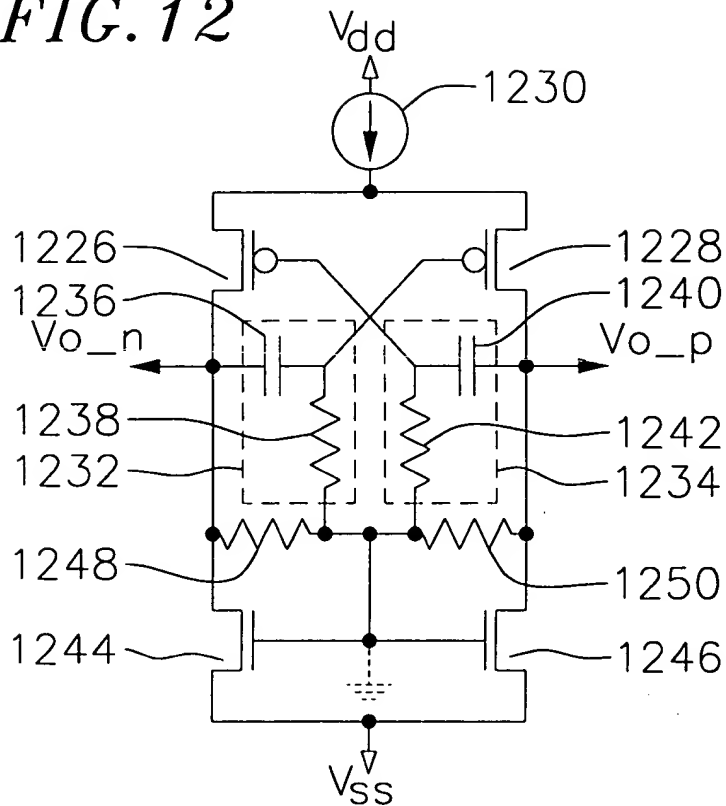
*FIG. 10*



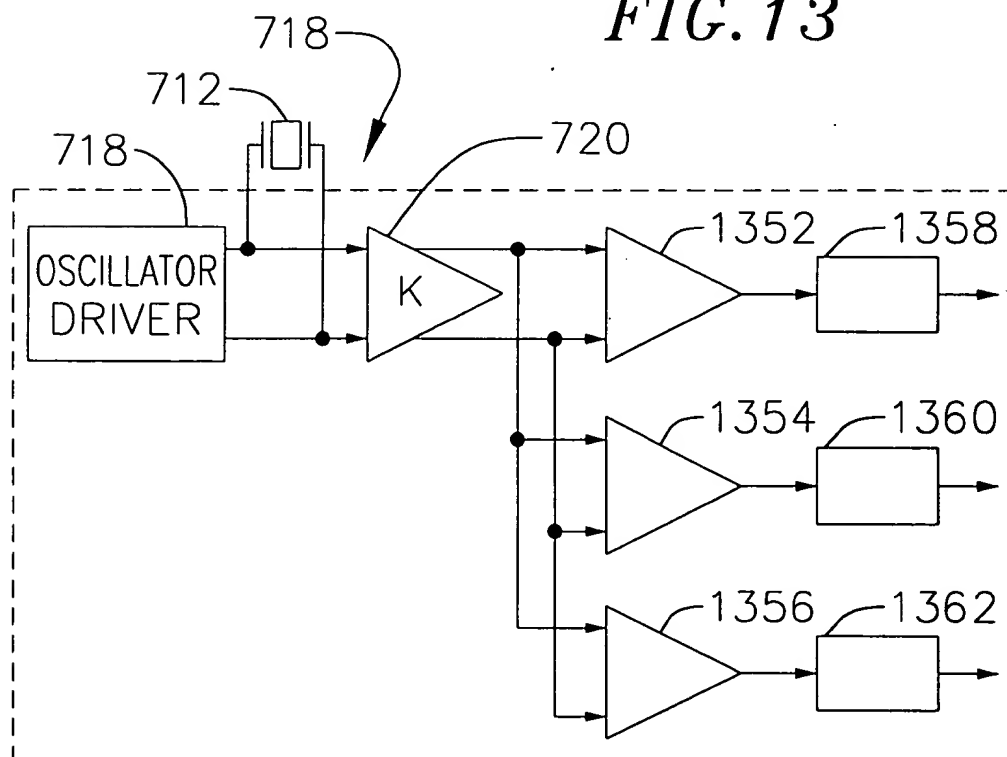
*FIG. 11*



**FIG. 12**



**FIG. 13**



*FIG. 14*

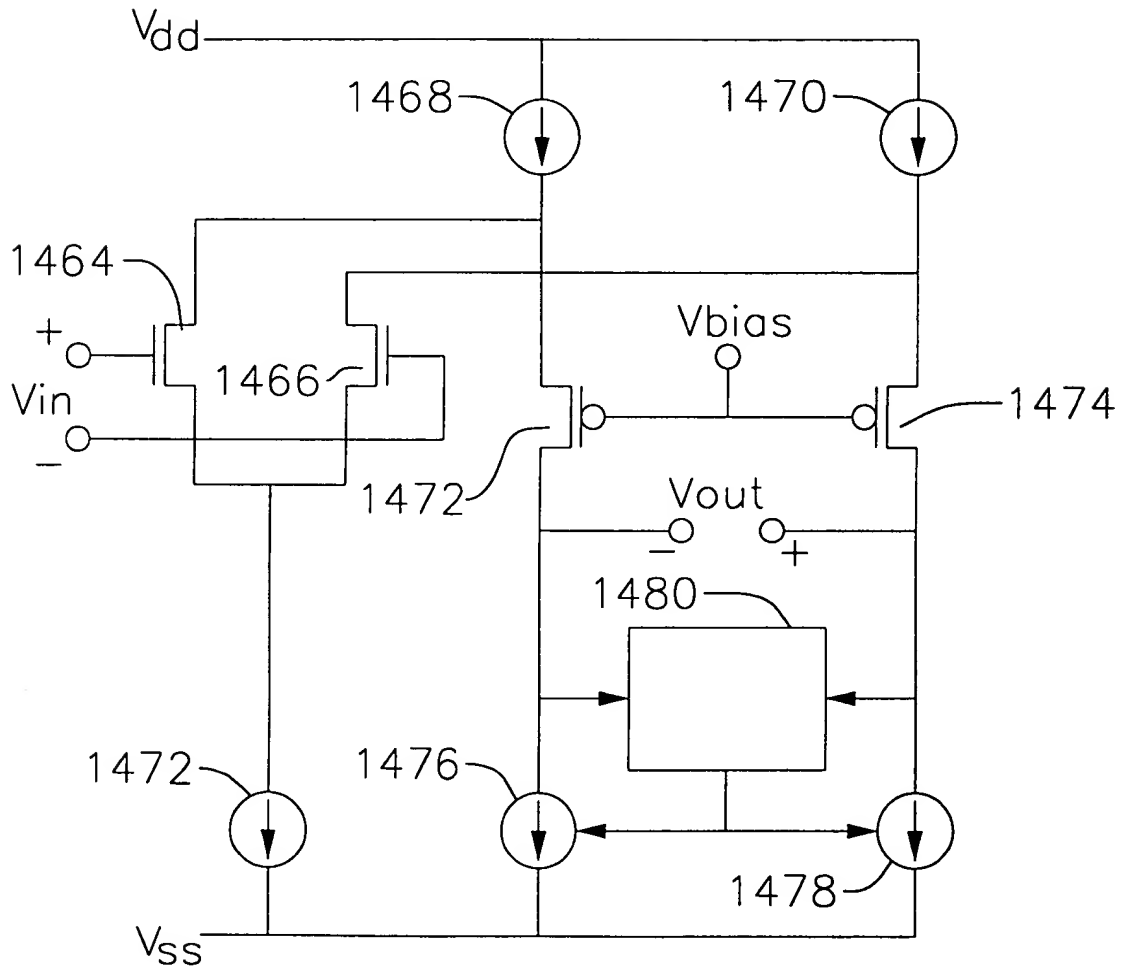






FIG. 15

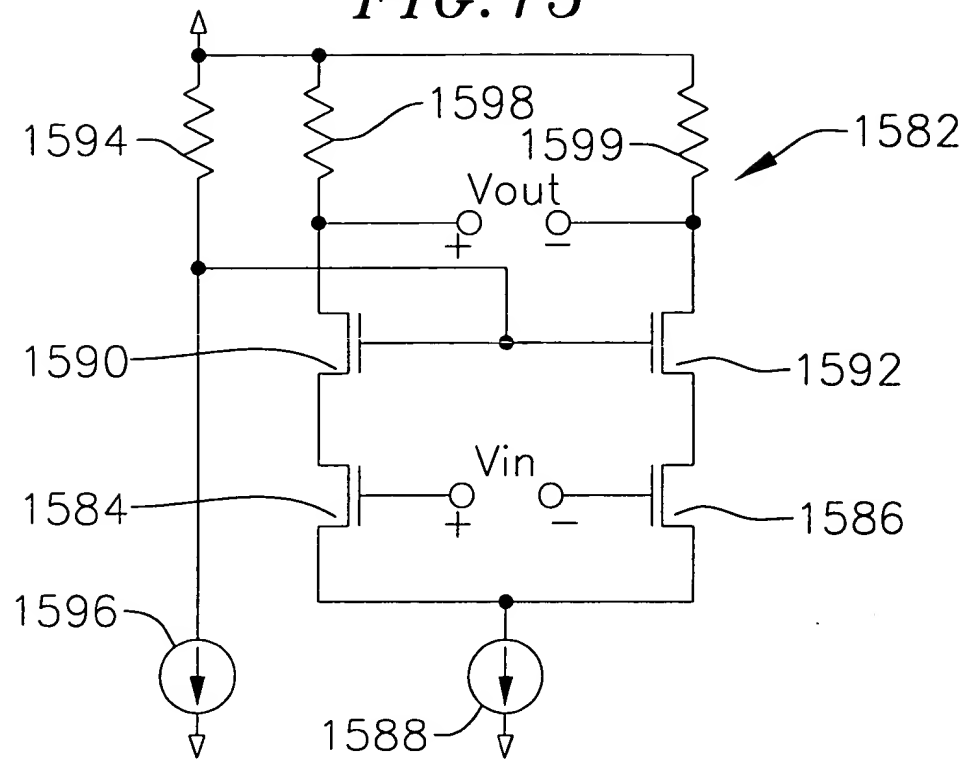
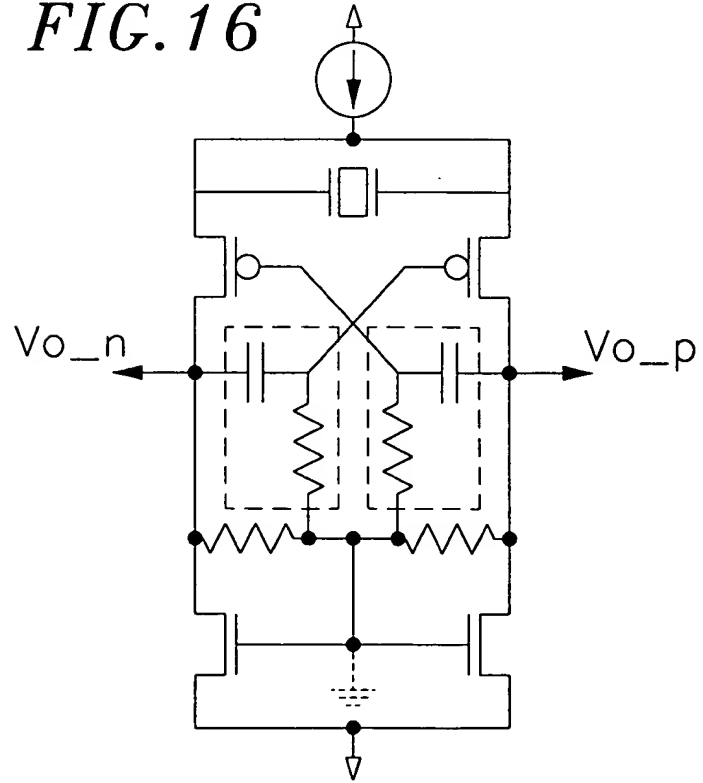
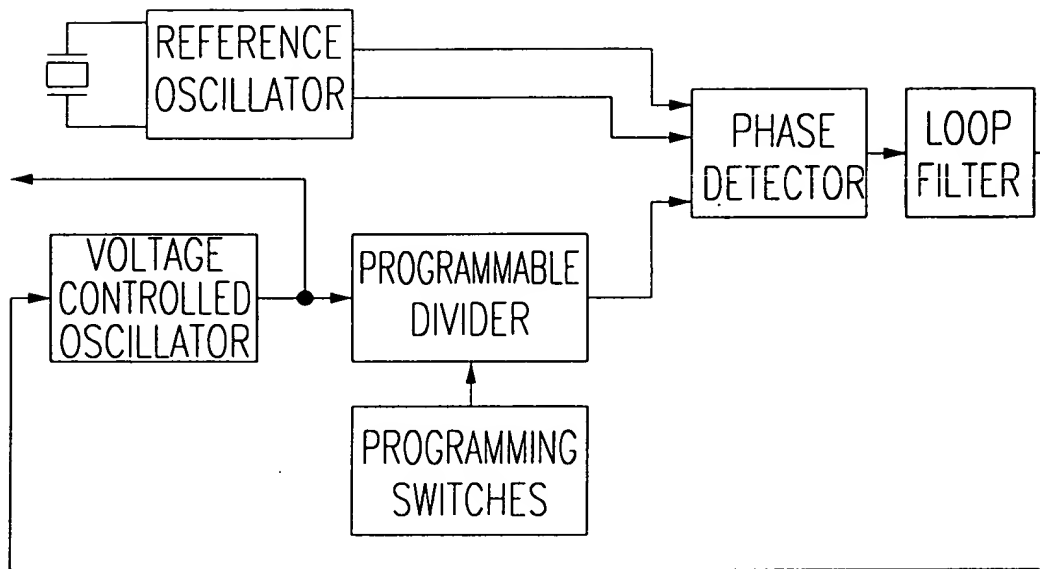


FIG. 16



2025 RELEASE UNDER E.O. 14176

*FIG. 17*



*FIG. 18*

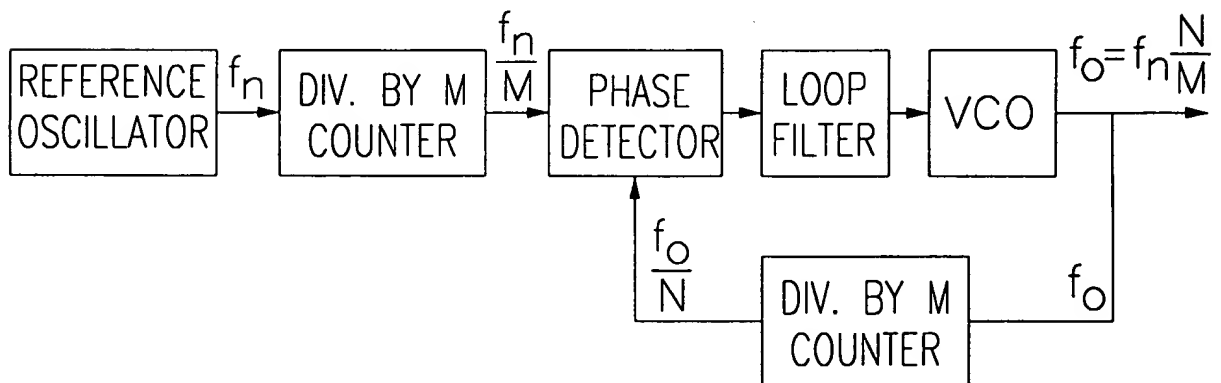


FIG. 19

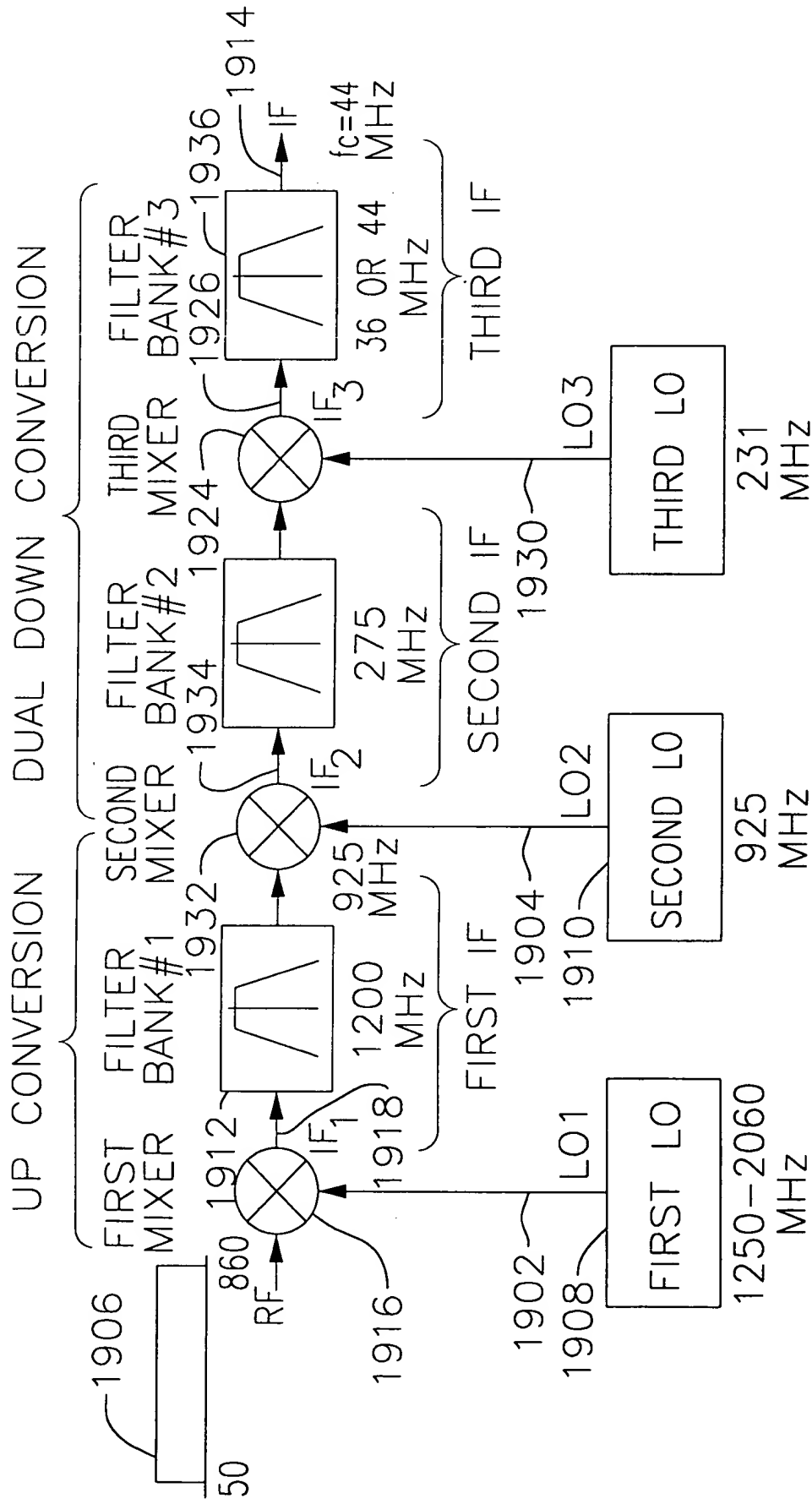
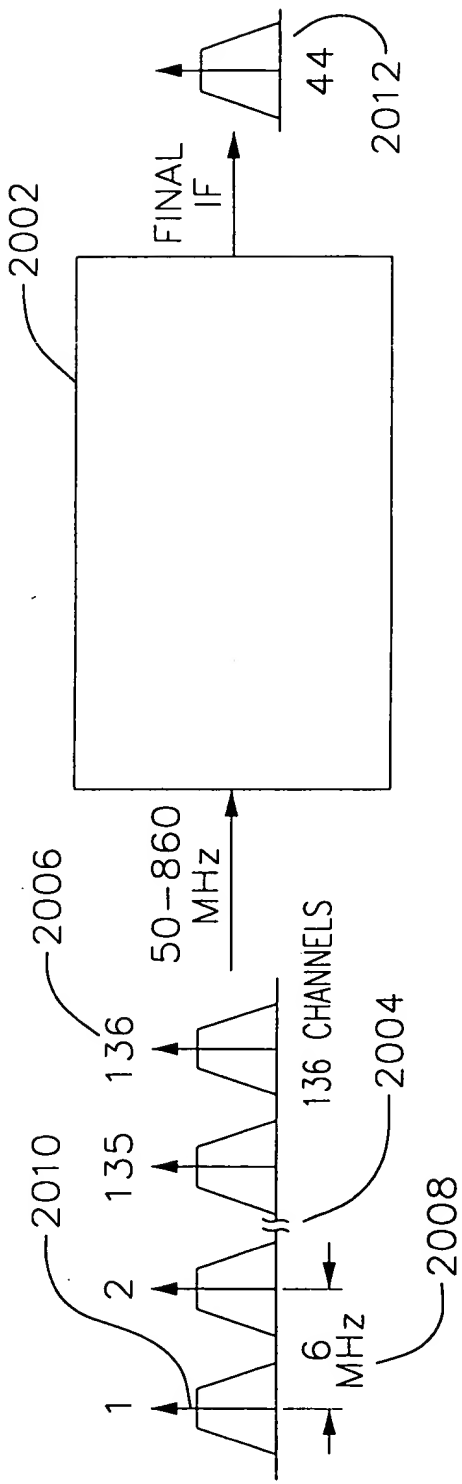


FIG. 20



PPL Xtol REFERENCE=10MHz  
 LO-1, 10MHz FREQUENCY STEPS  
 LO-2, 100kHz FREQUENCY STEPS

# FIG.21

44MHz IF

NOTE  
 • LO-2 REF=100KHz  
 SO DIVIDE RANGE=9216 TO 9280

TABLE OF FREQUENCIES BASED ON  
 COARSE/FINE PLL SOLUTION:

Fr (MHz)	50	56	62	68	74	80	86	92	98	104	110	116	122	128	"	854	860
LO-1 (MHz)	1250	1260	1260	1270	1270	1280	1290	1290	1300	1300	1310	1320	1320	1330	"	2050	2060
IF-1 (MHz)	1200	1204	1198	1202	1196	1200	1204	1198	1202	1196	1200	1204	1198	1202	"	1196	1200
LO-2 (MHz)	924.8	928.0	923.2	926.4	921.6	924.8	928.0	923.2	926.4	921.6	924.8	928.0	923.2	926.4	"	921.6	924.8
IF-2 (MHz)	275.2	276	274.8	275.6	274.4	275.2	276.0	274.8	275.6	274.4	275.2	276.0	274.8	275.6	"	274.4	275.2
LO-3 (MHz)	231.2	232	230.8	232	230	231	232	231	232	230	231	232	231	232	"	230	231
IF-3 (MHz)	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	"	44.0	44.0



FIG.23

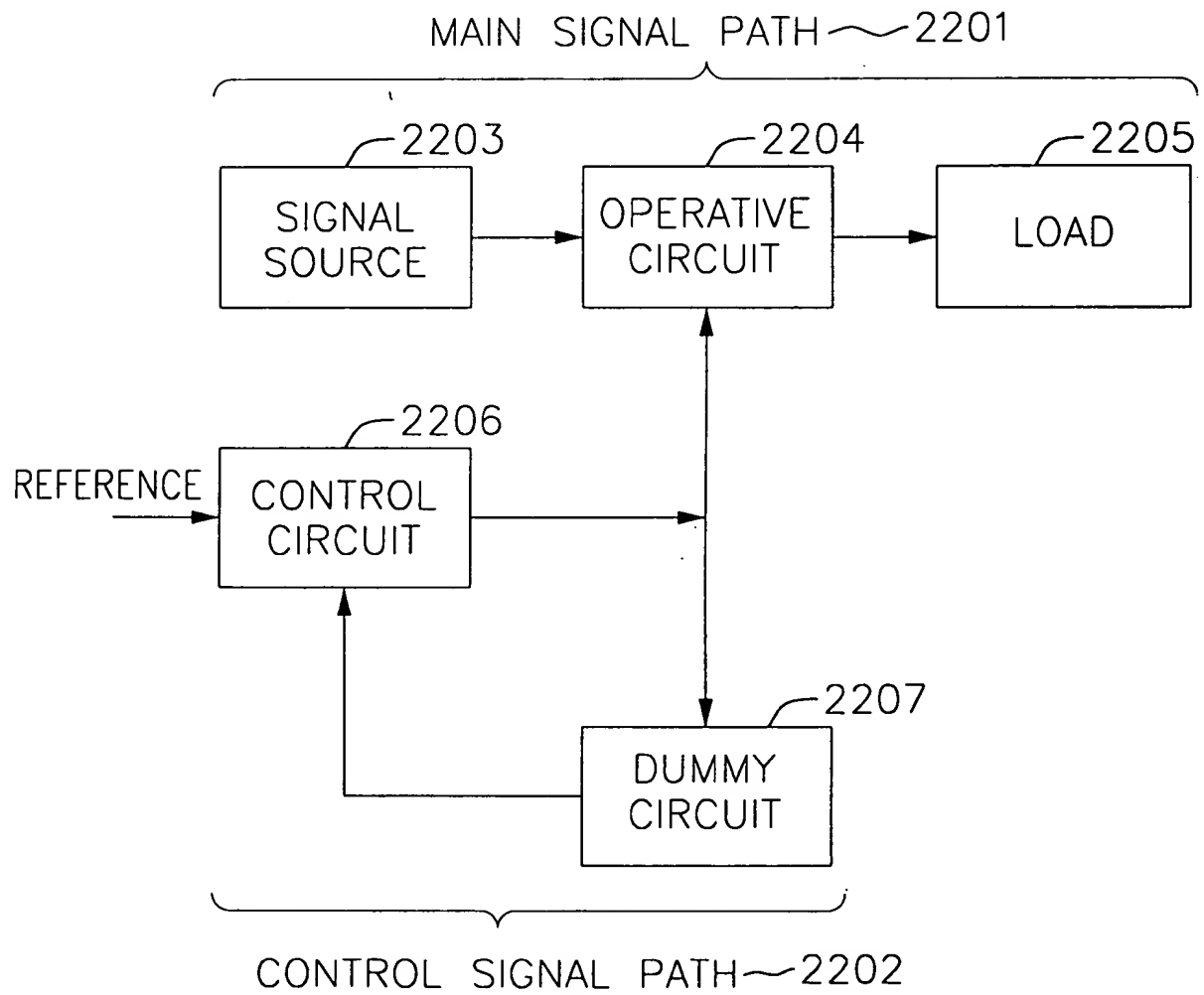


FIG. 24a

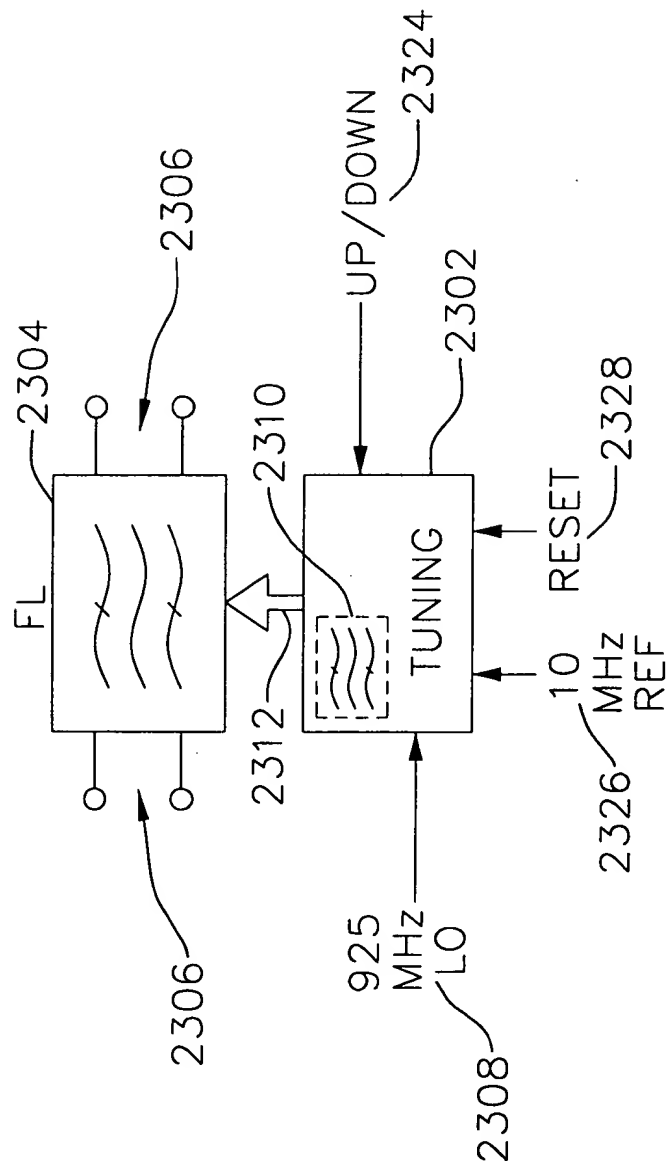




FIG. 24b

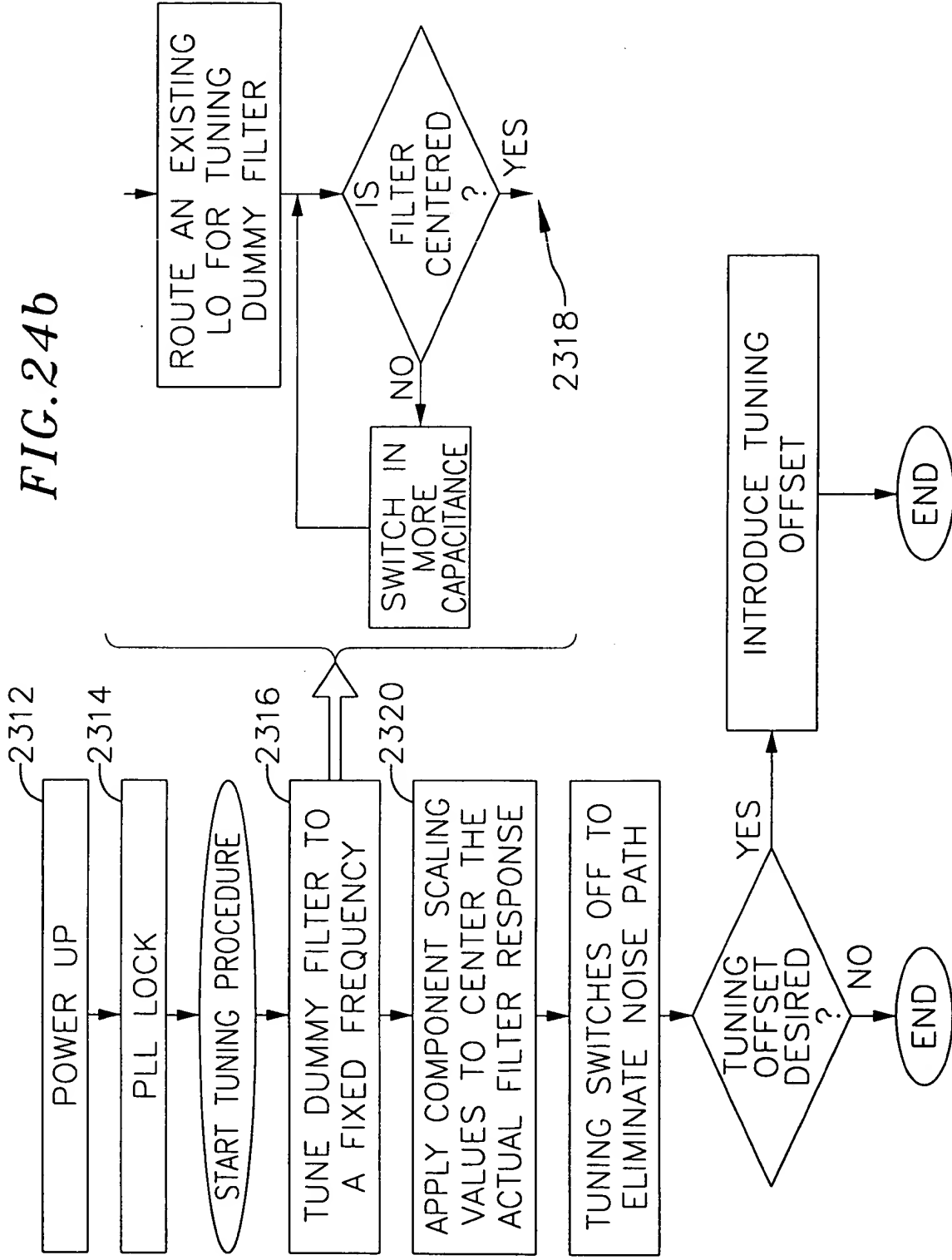


FIG. 24c

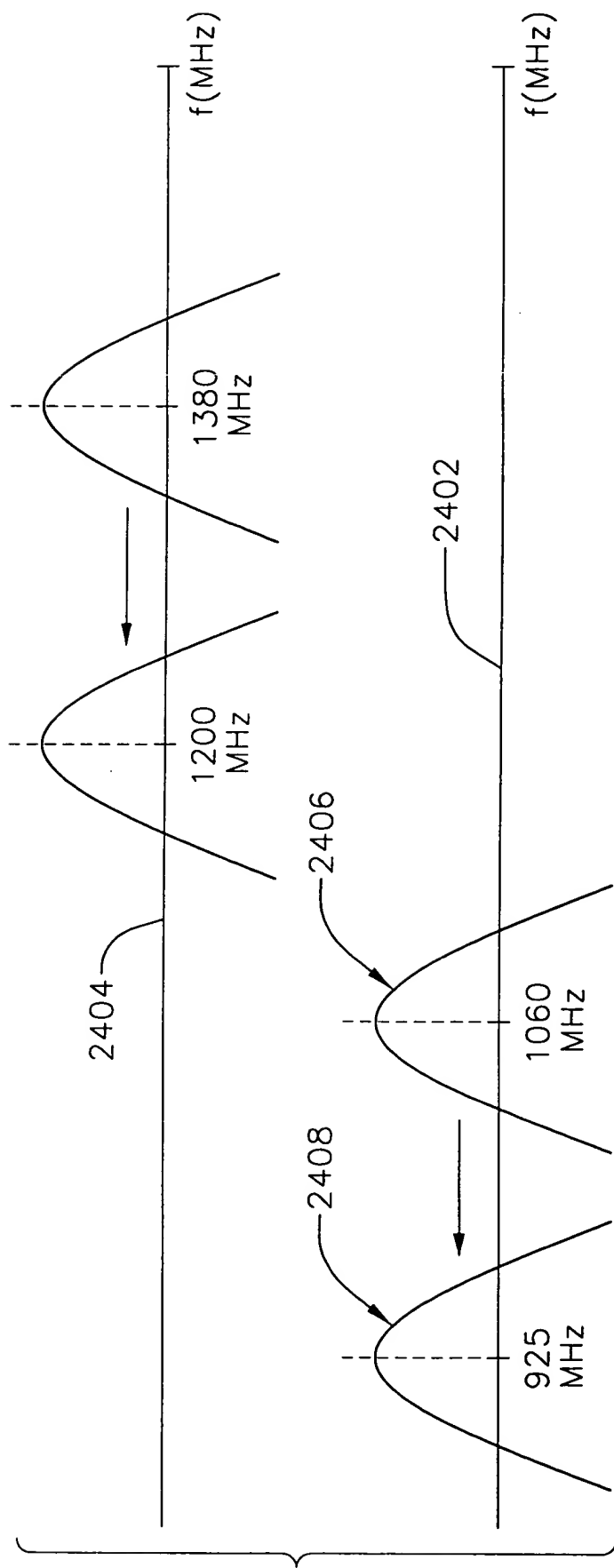


FIG. 25

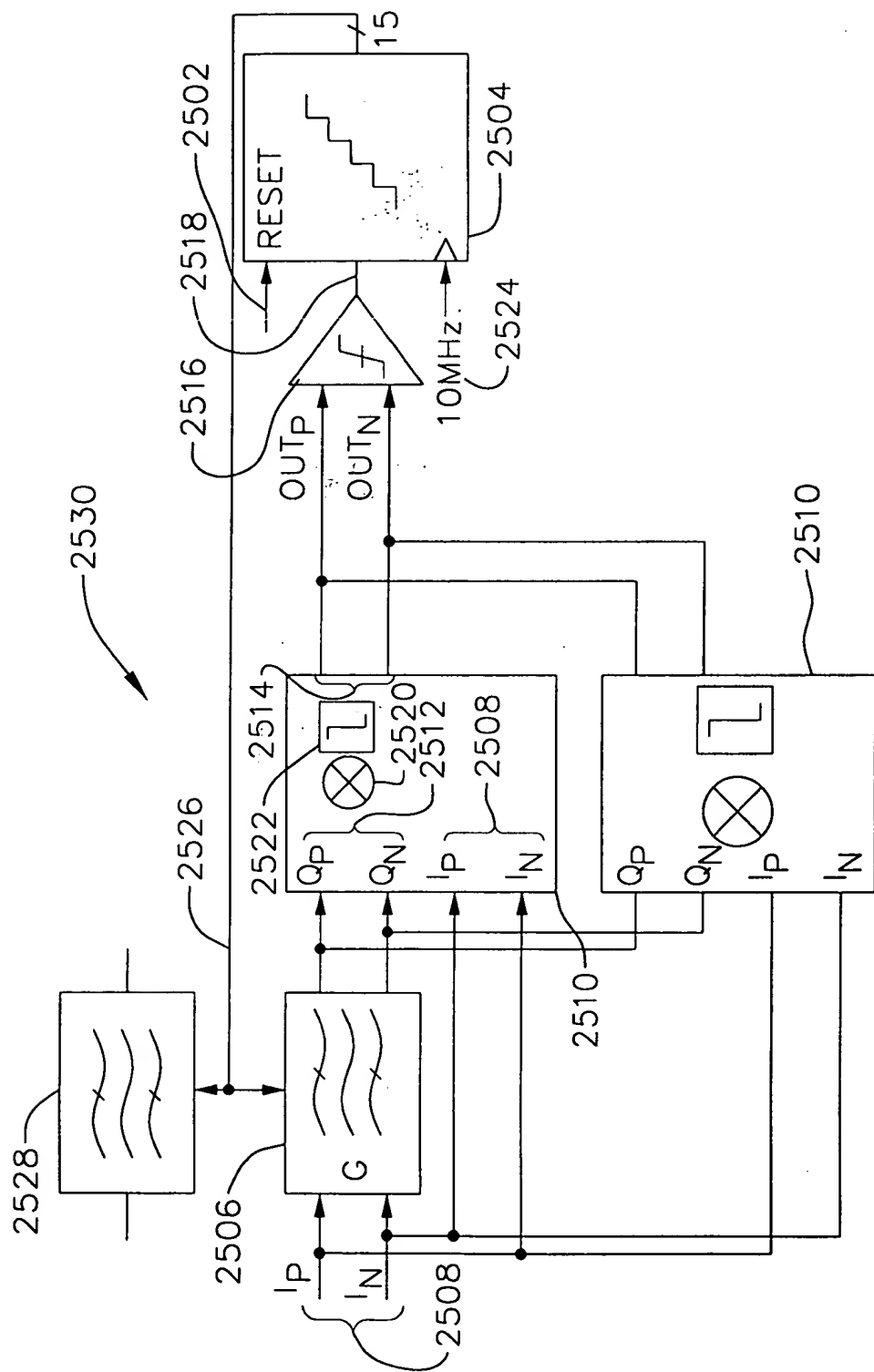


FIG. 26

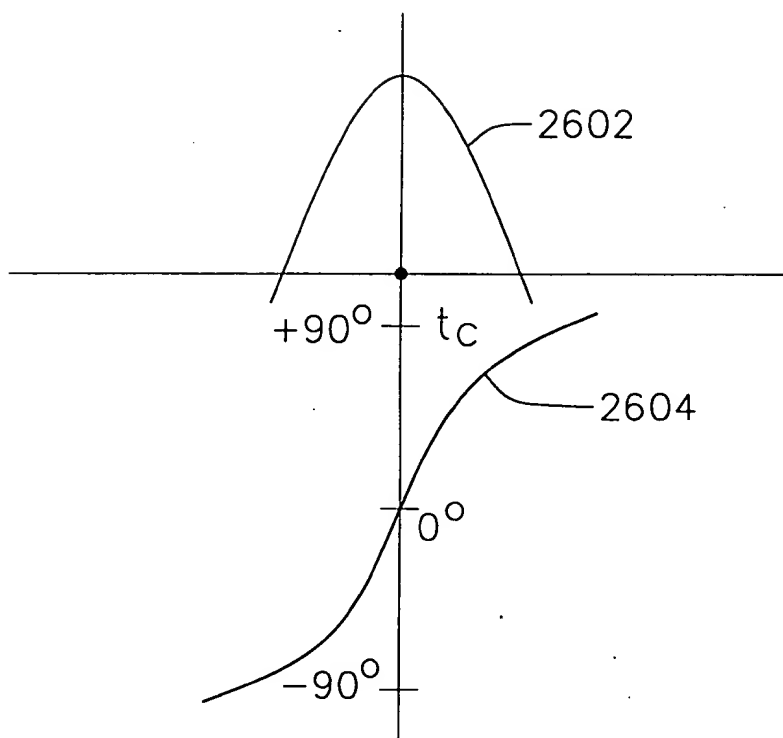


FIG. 27

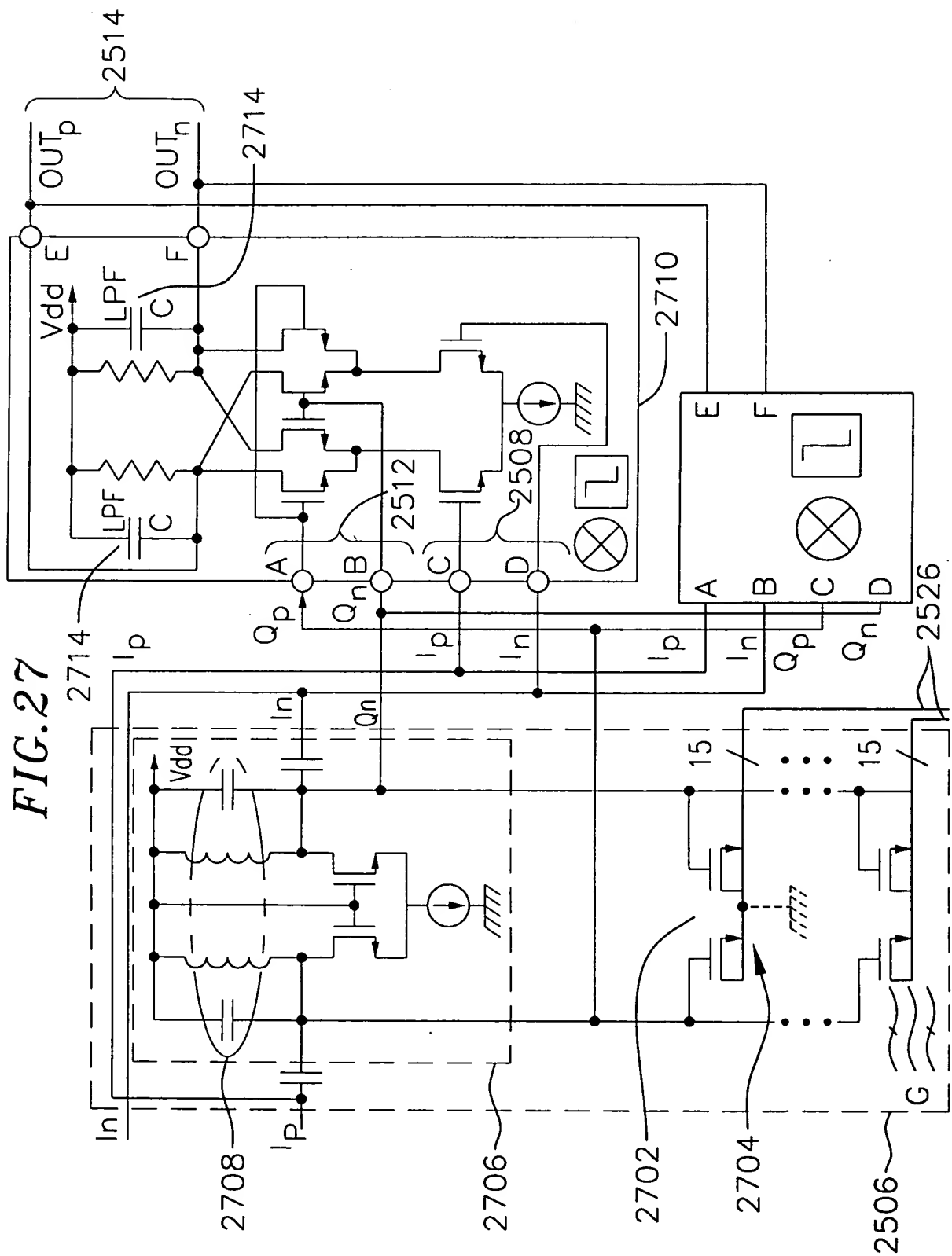


FIG. 28a

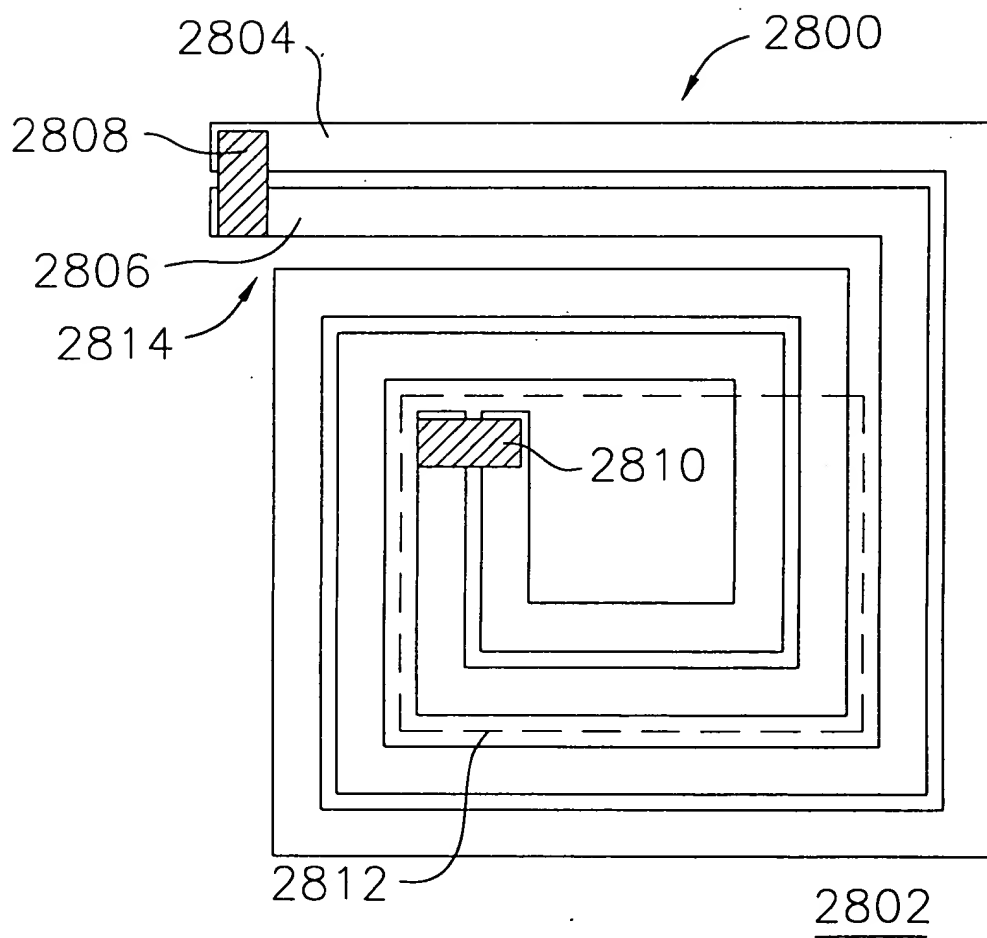




FIG.28b

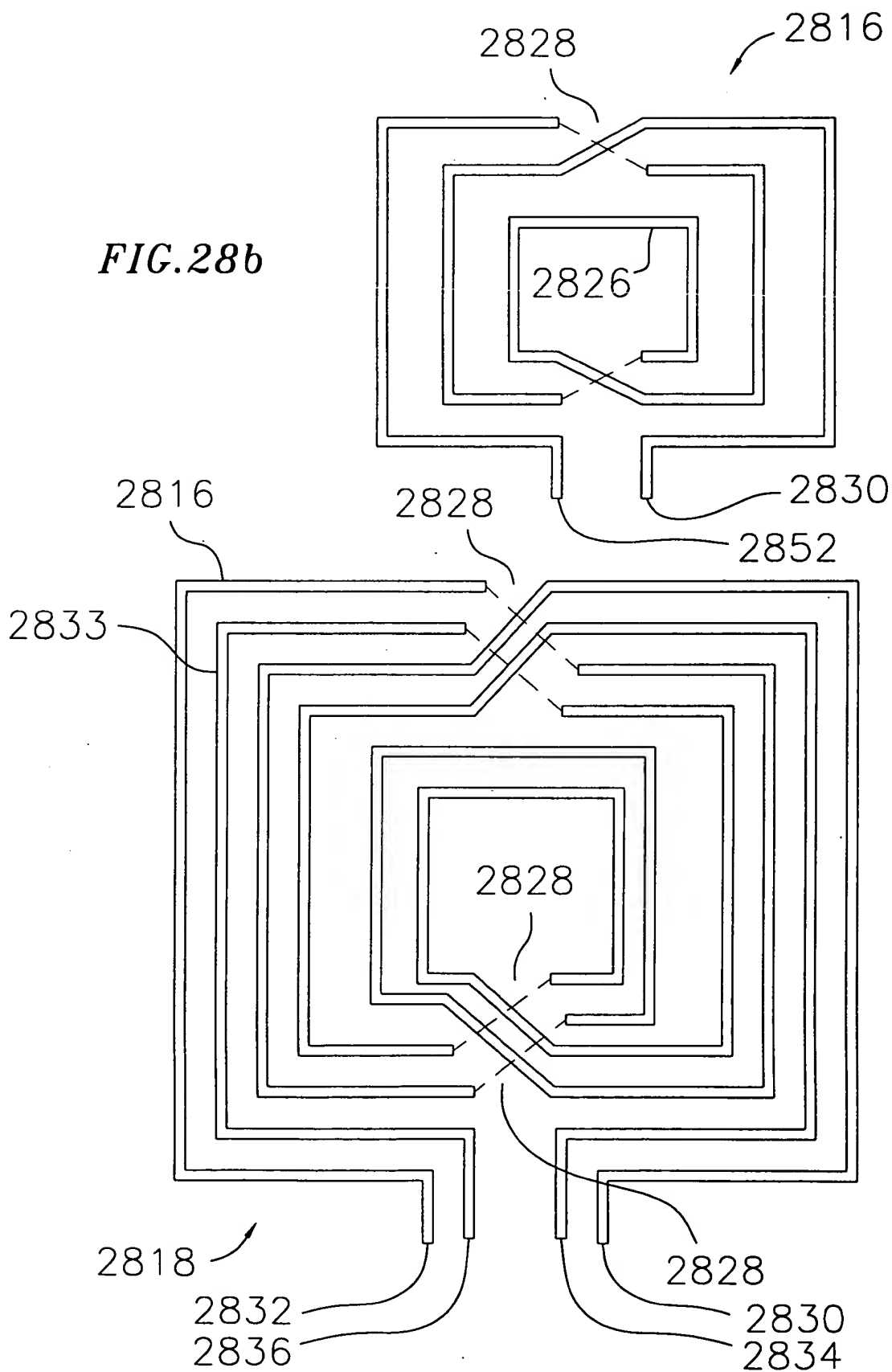


FIG. 28c

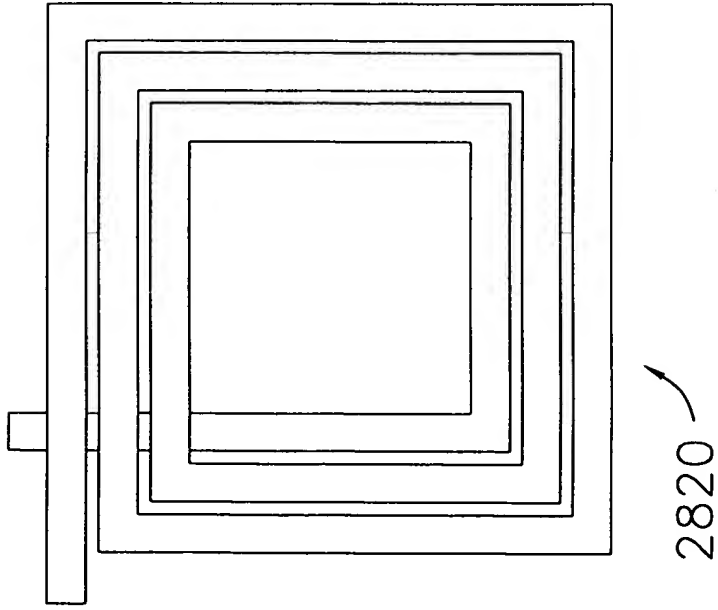


FIG. 28d

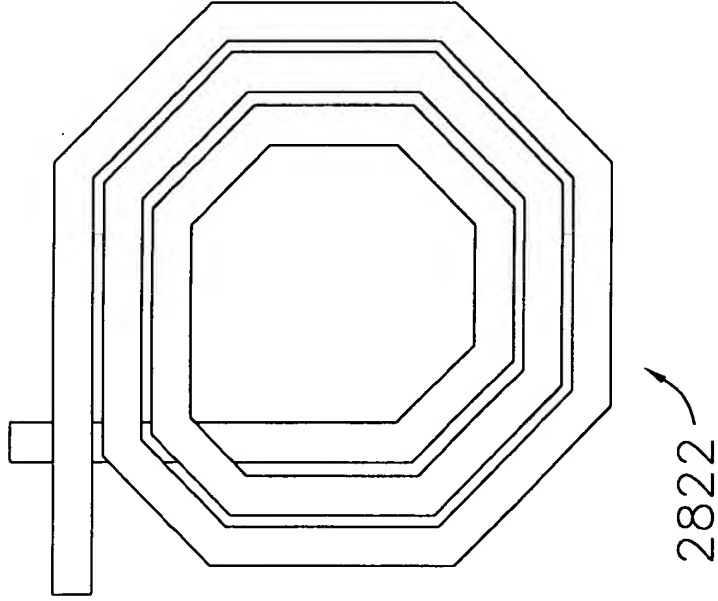
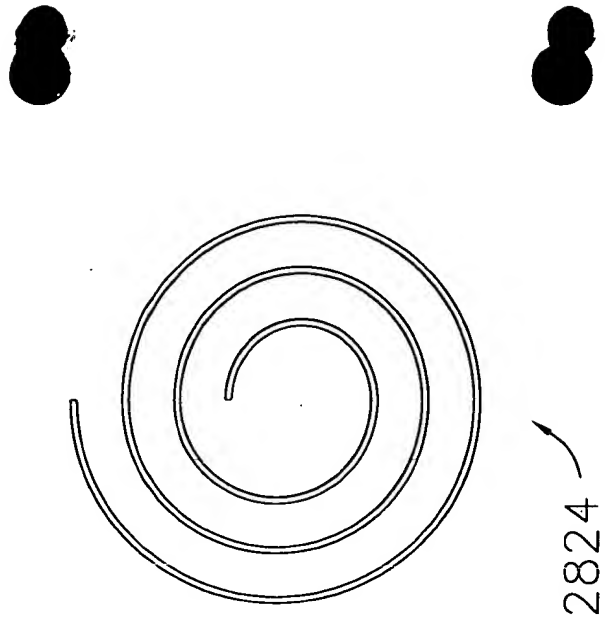
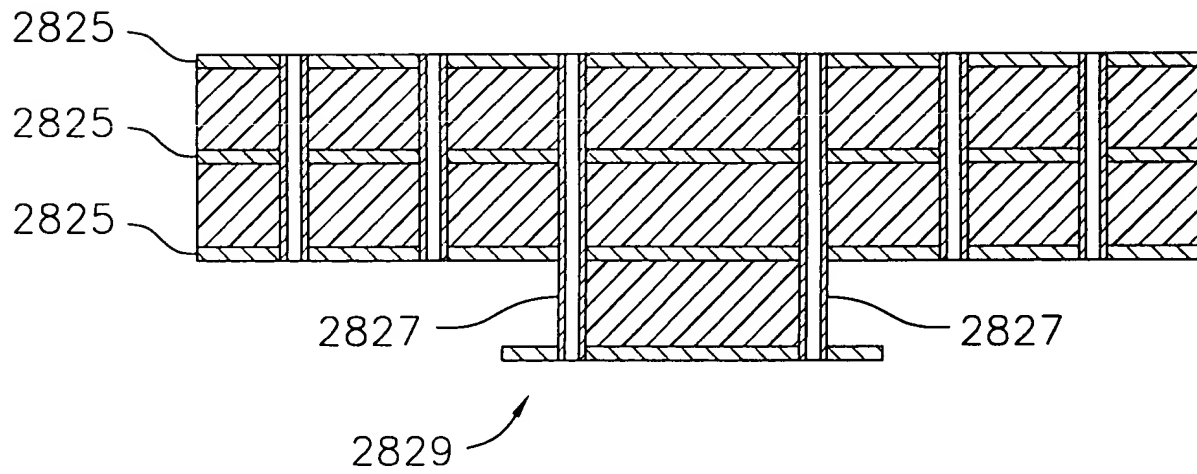


FIG. 28e





*FIG. 28f*



*FIG. 28g*

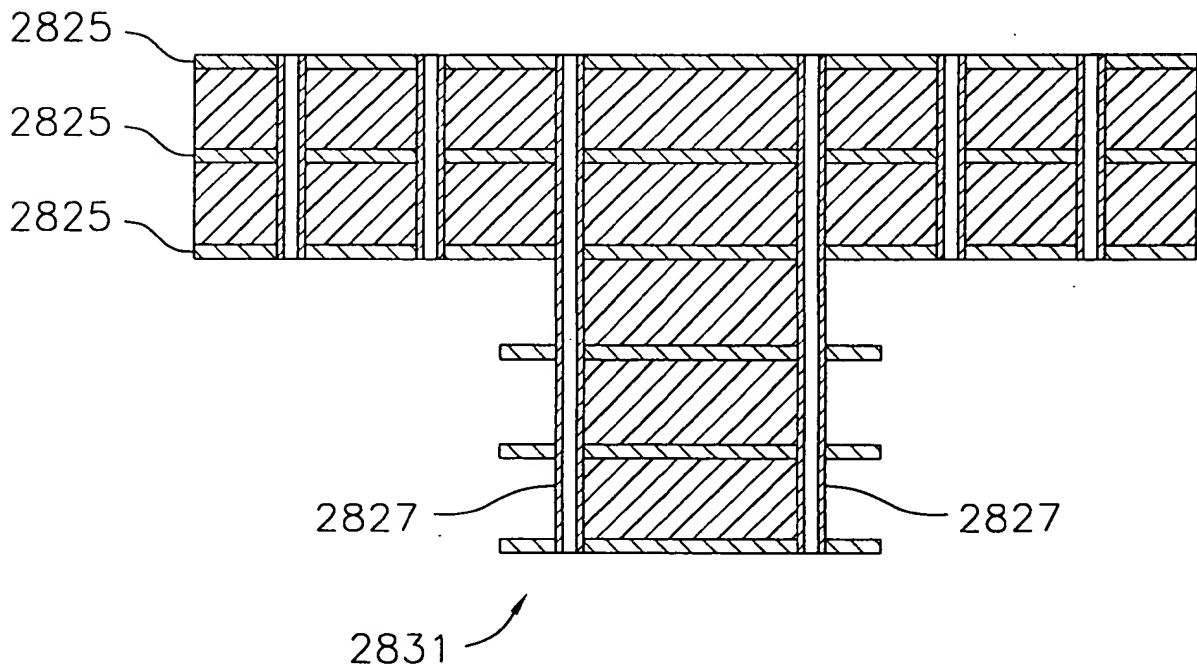
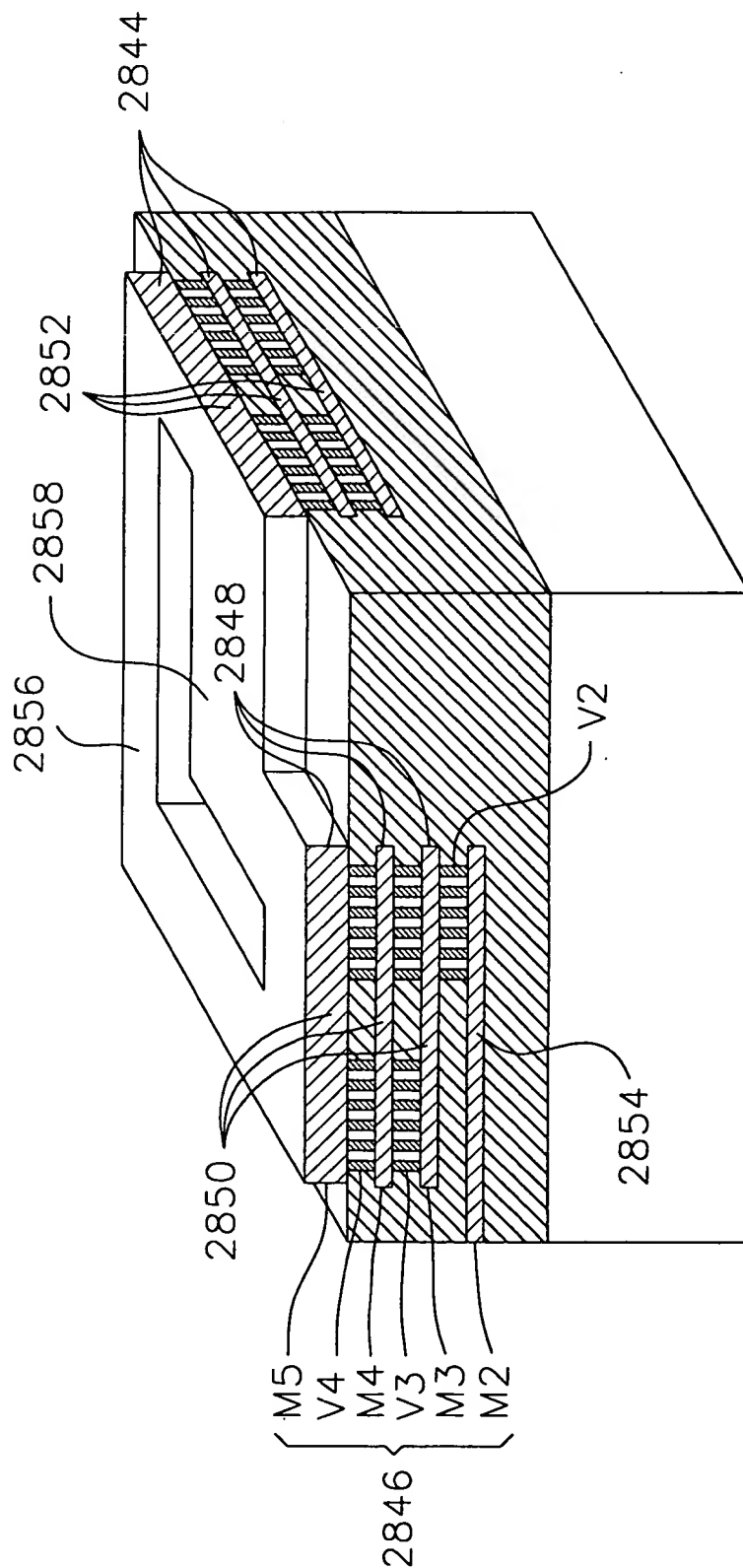


FIG. 28i



*FIG.28h*

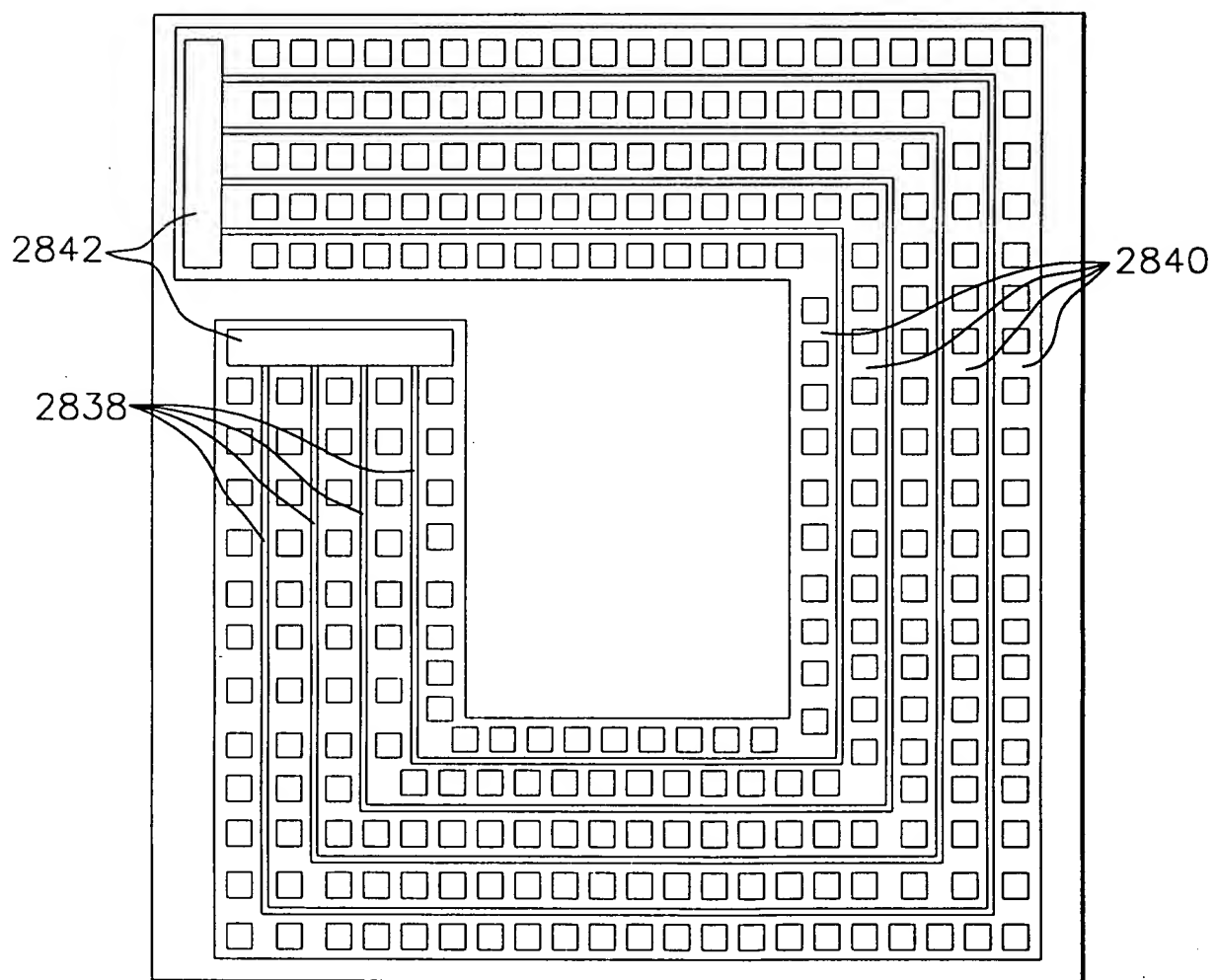


FIG. 28j

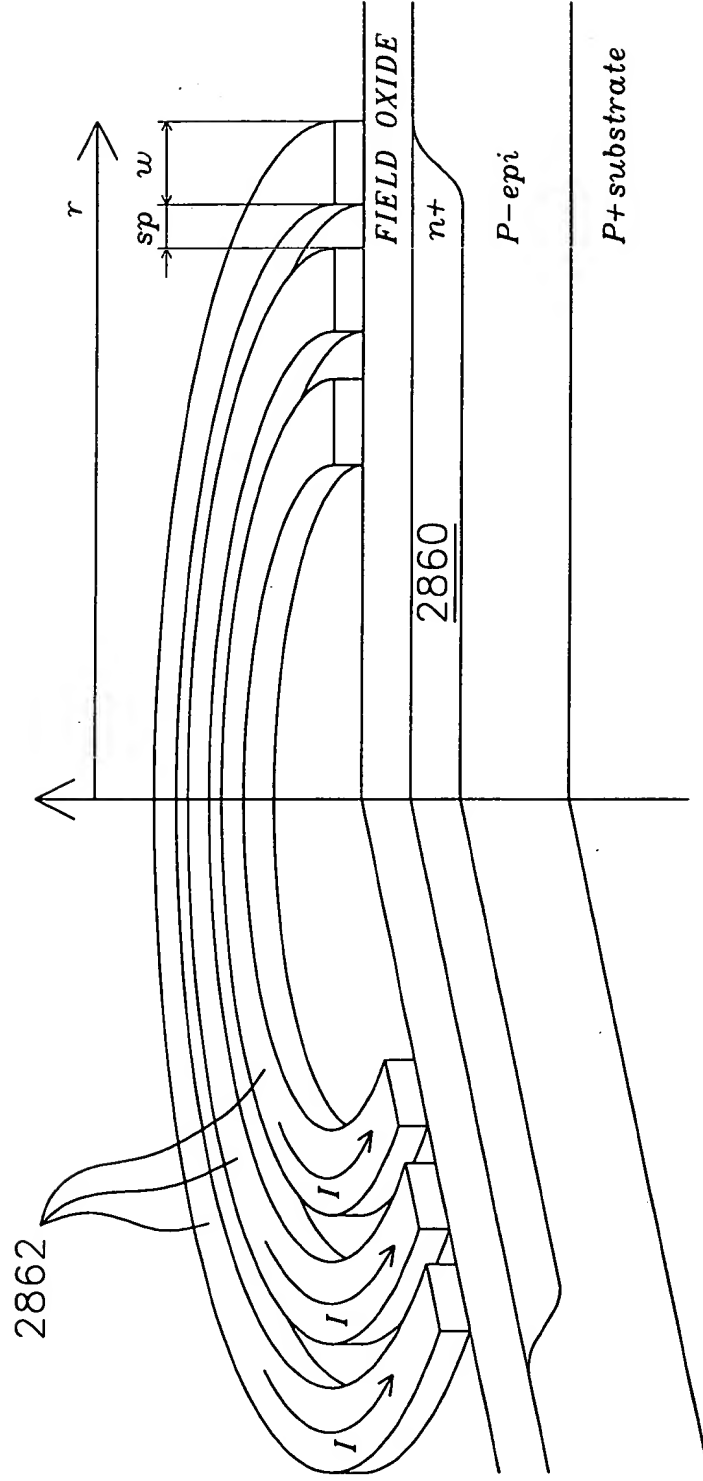


FIG. 28k

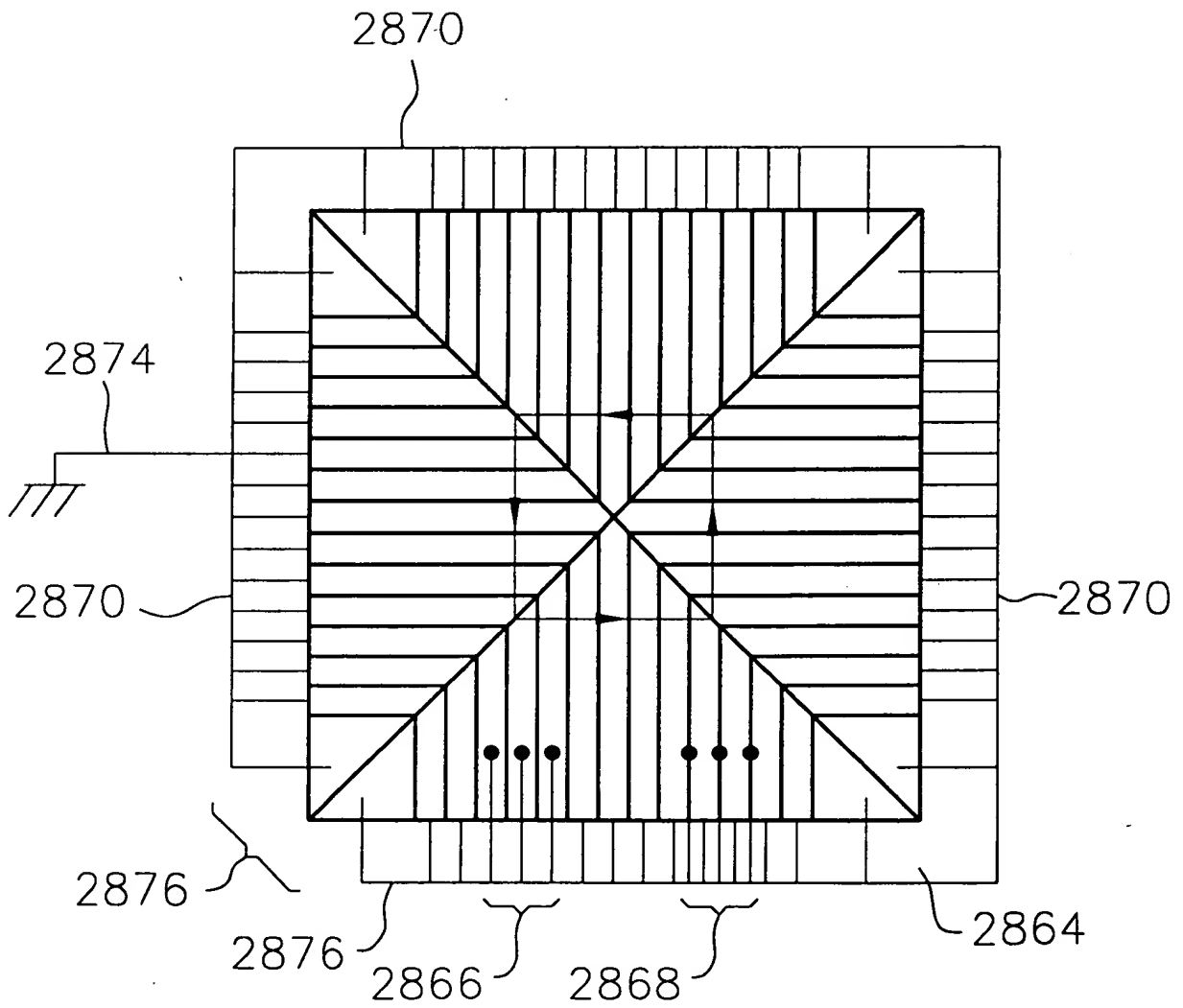


FIG.29

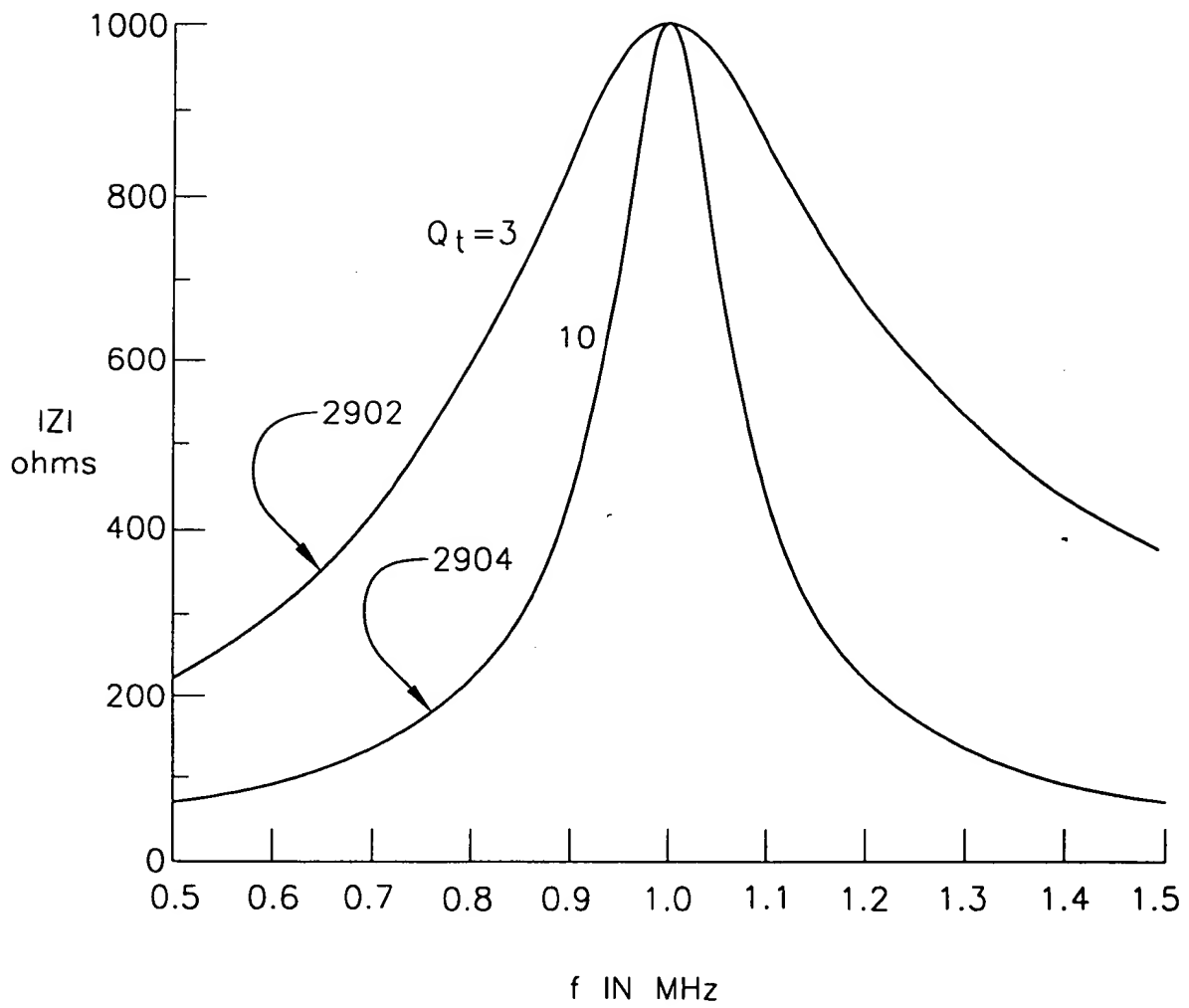




FIG.30

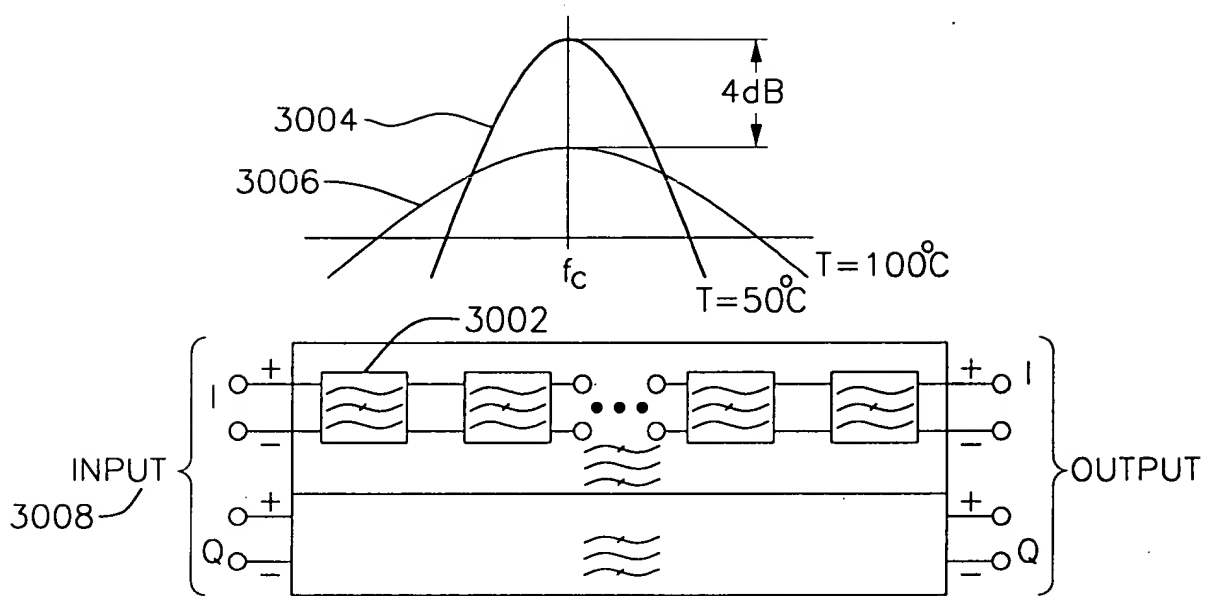


FIG.31a

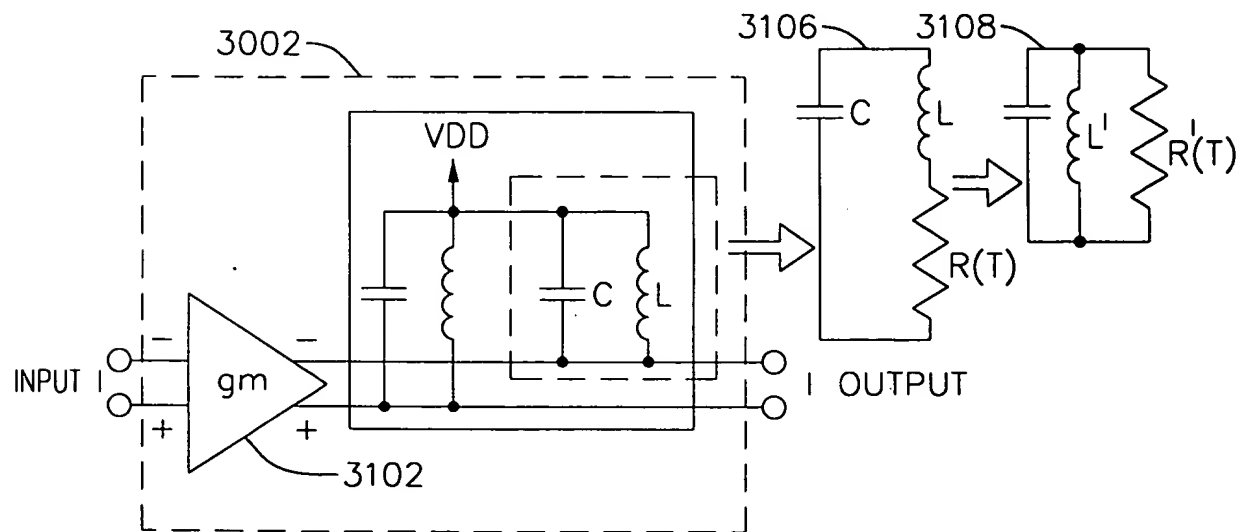
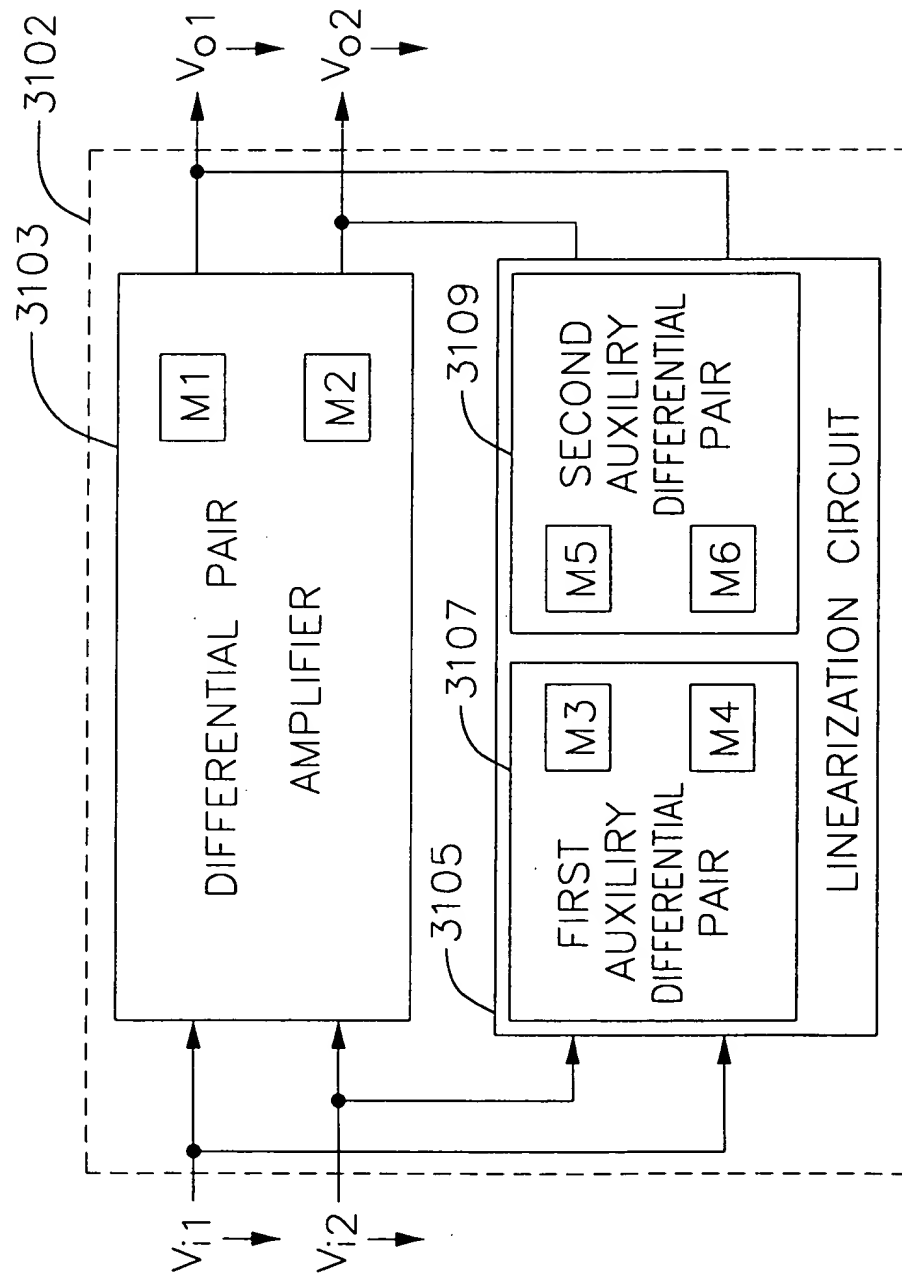


FIG. 31b





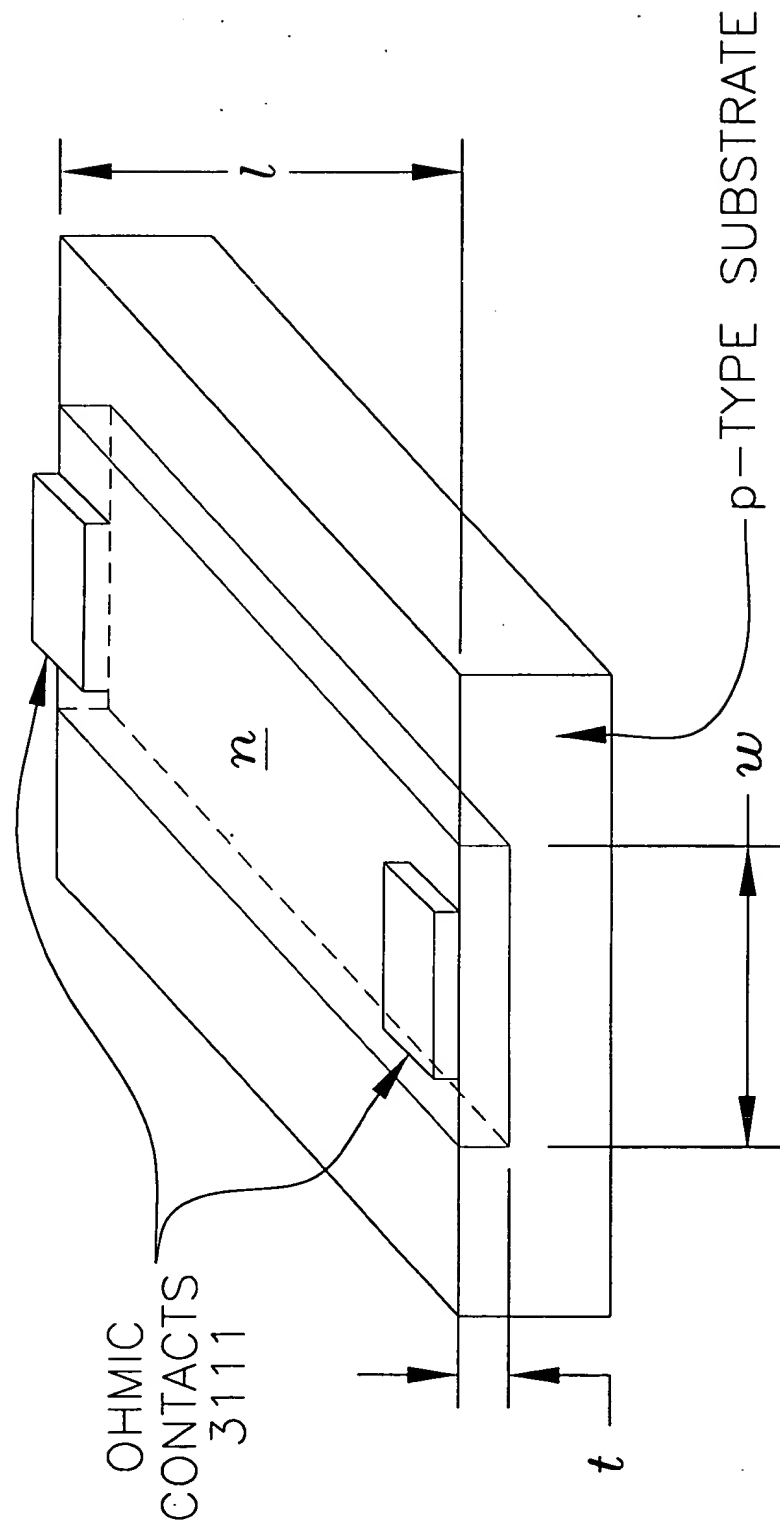
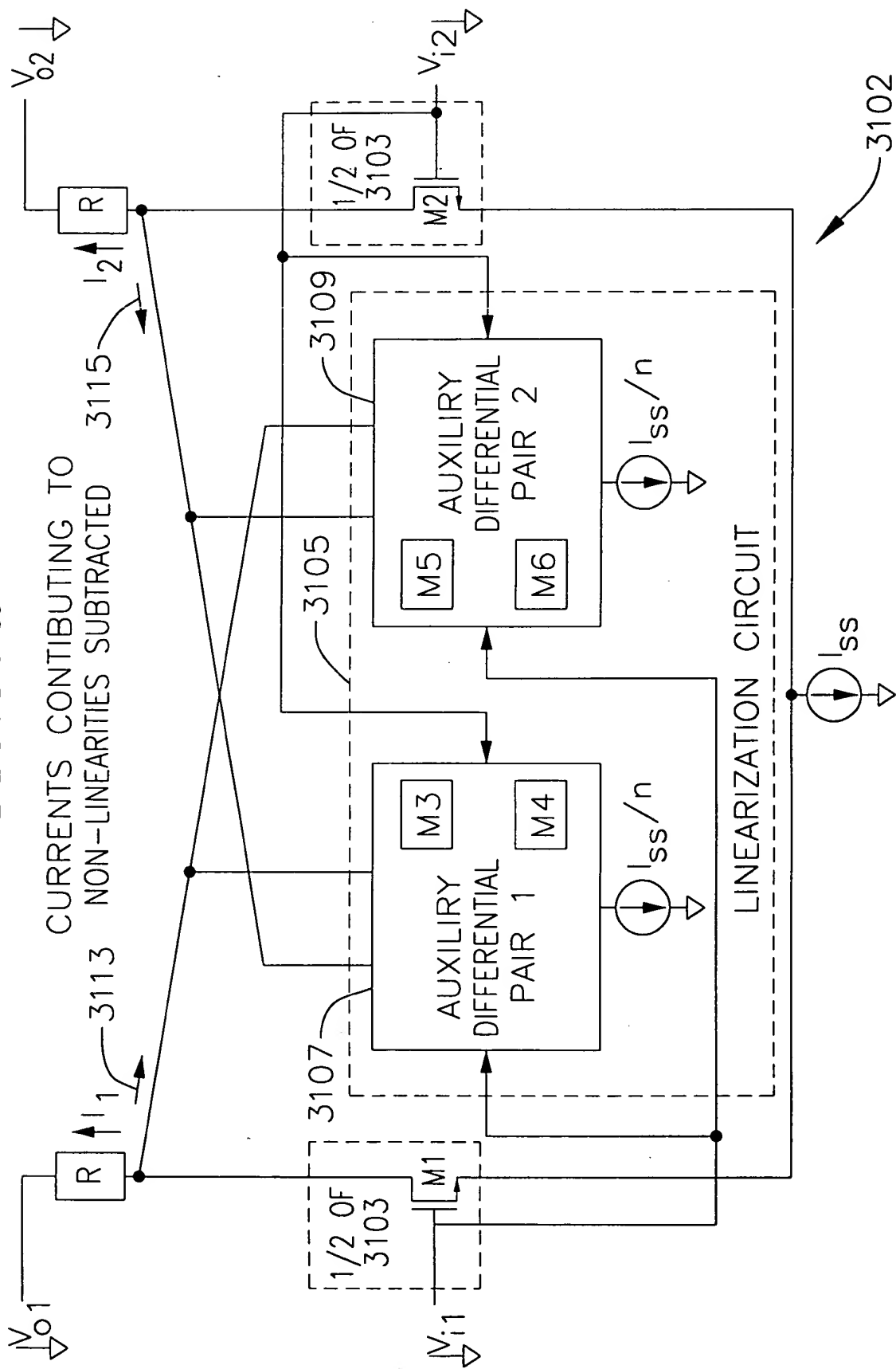


FIG. 31c

FIG. 31d





*FIG. 31e*

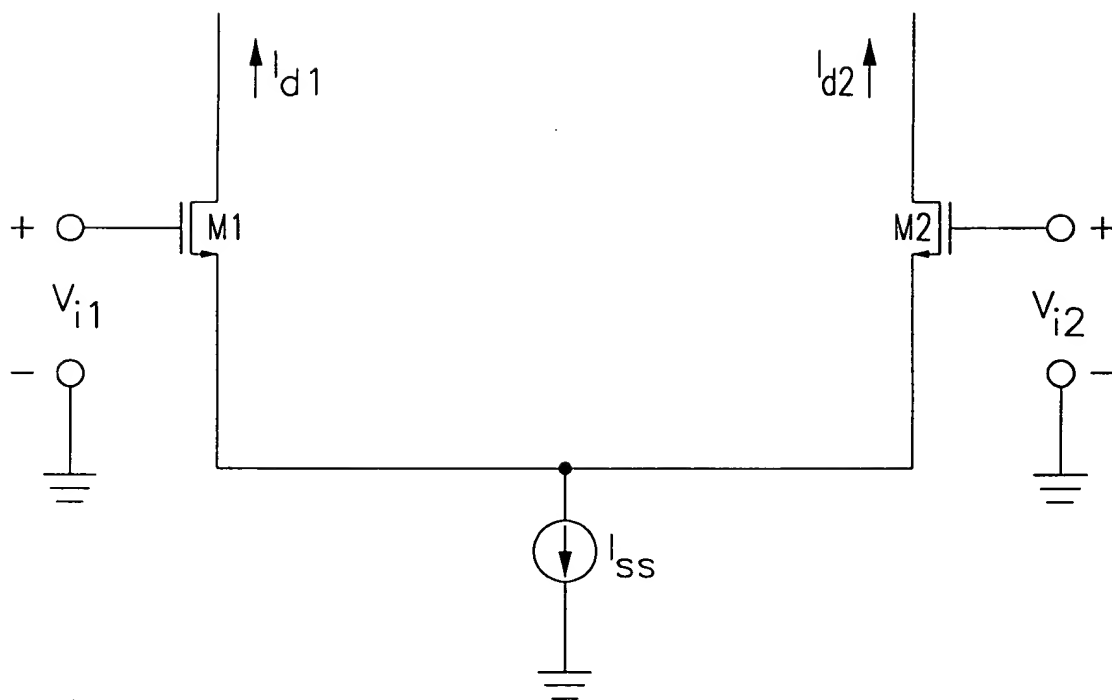


FIG. 31f

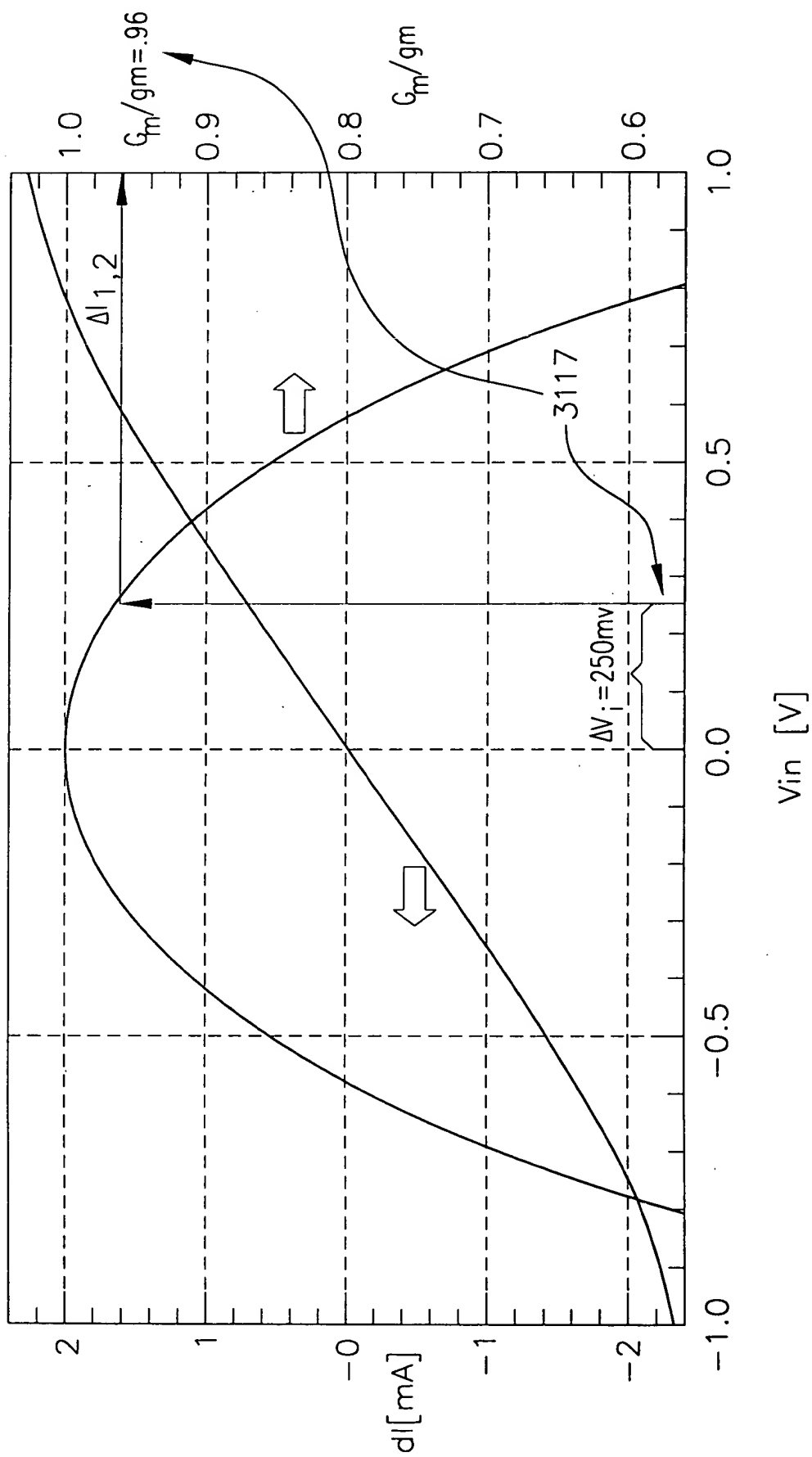


FIG. 31g

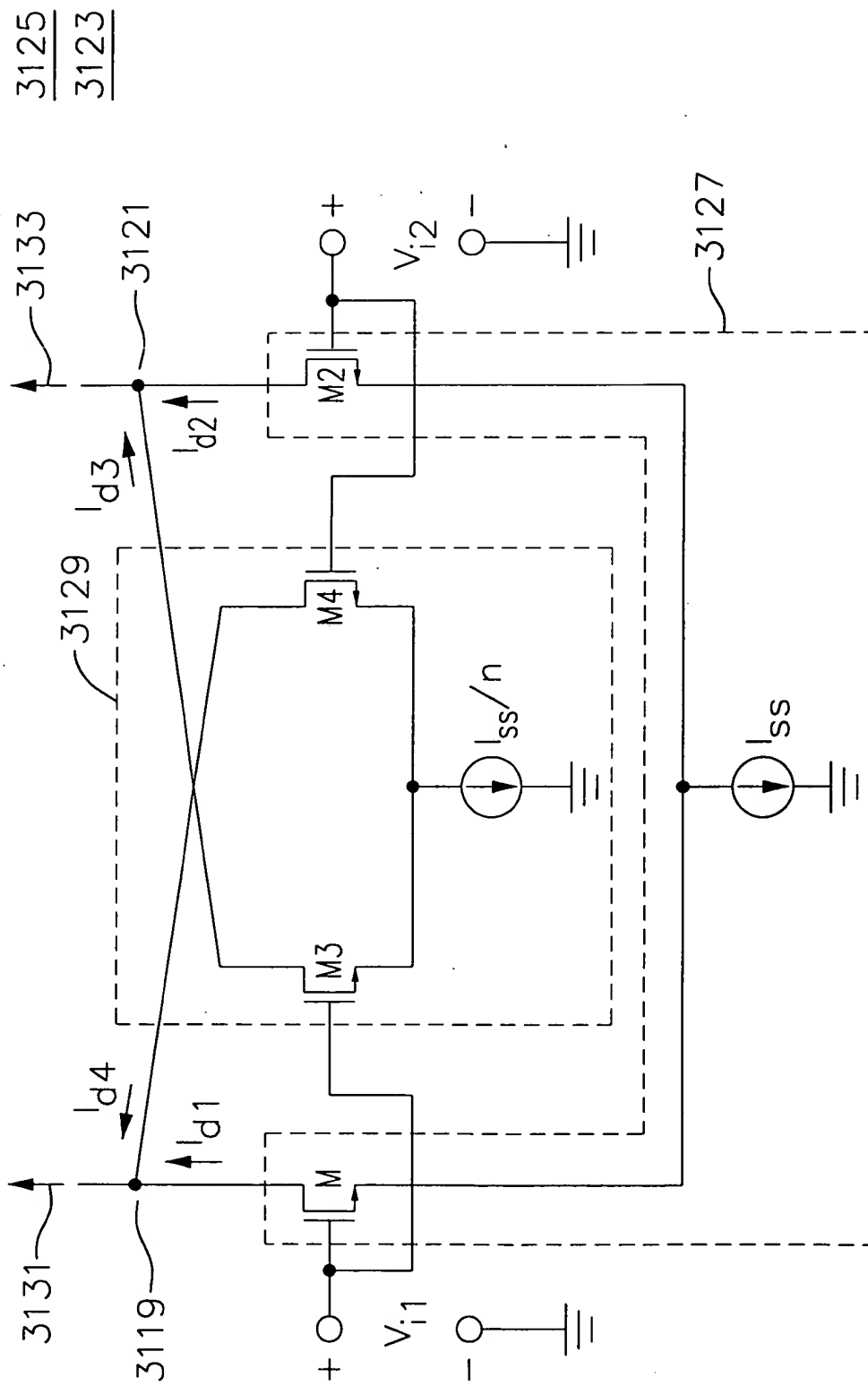
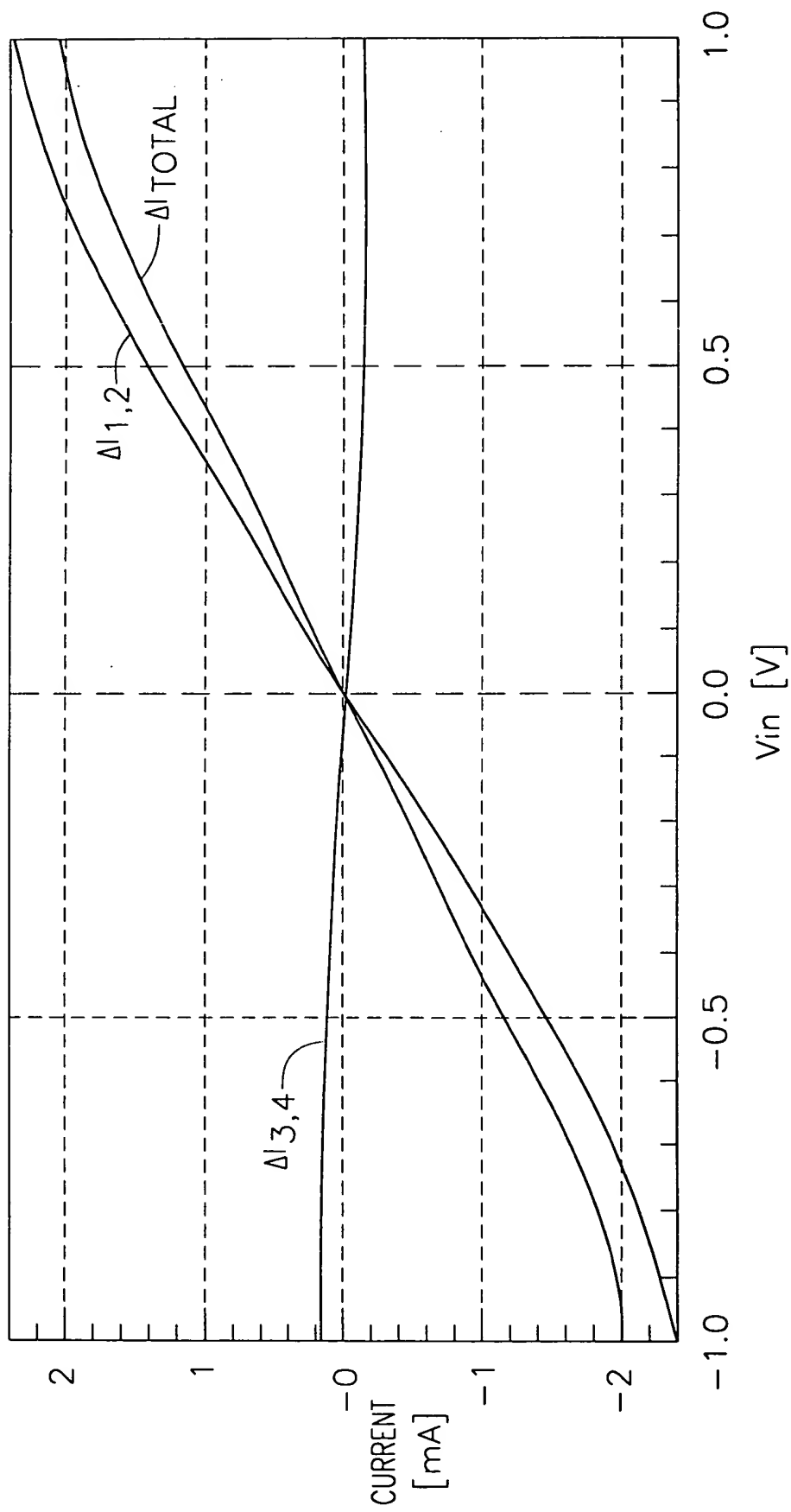


FIG. 31h



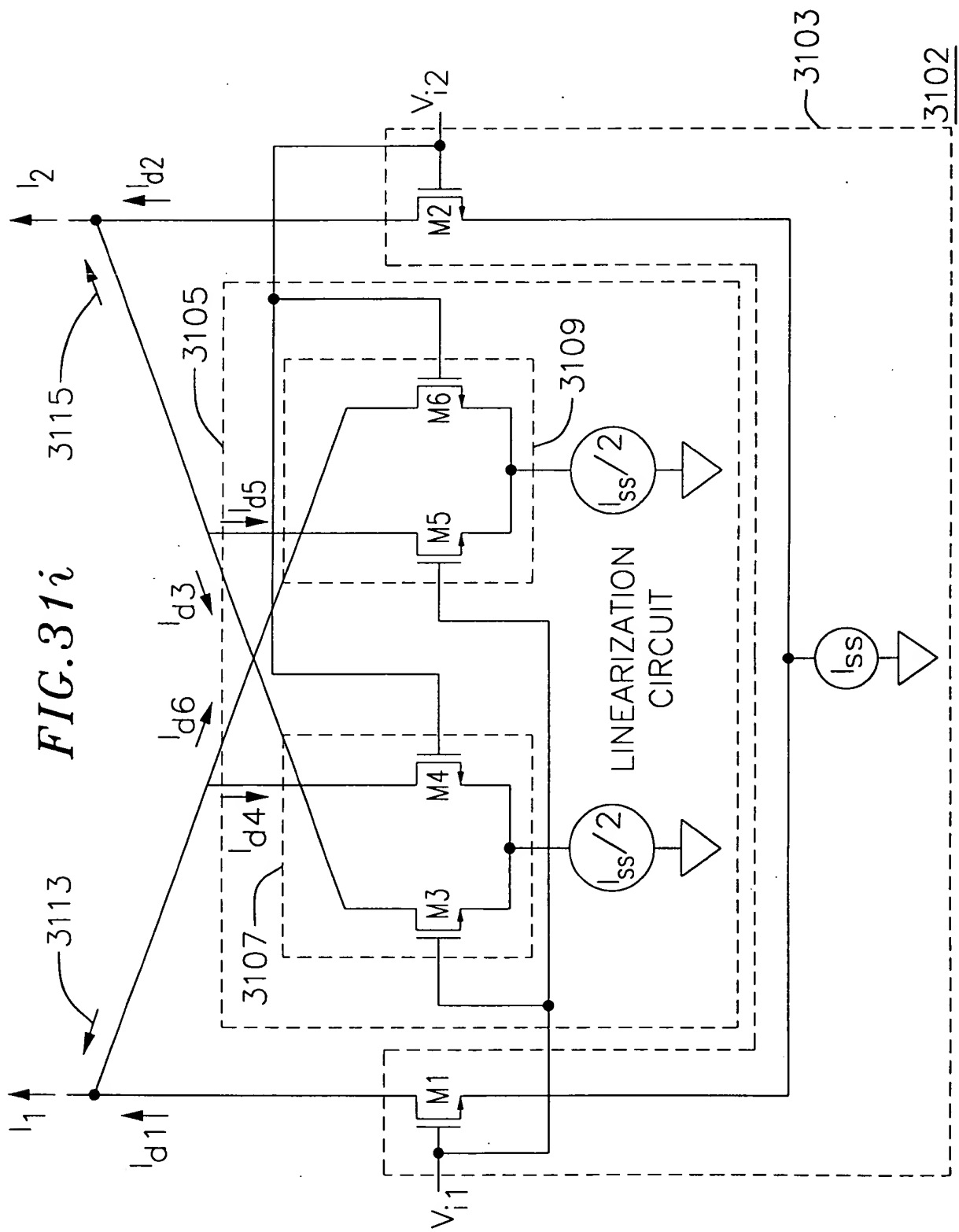


FIG. 31j

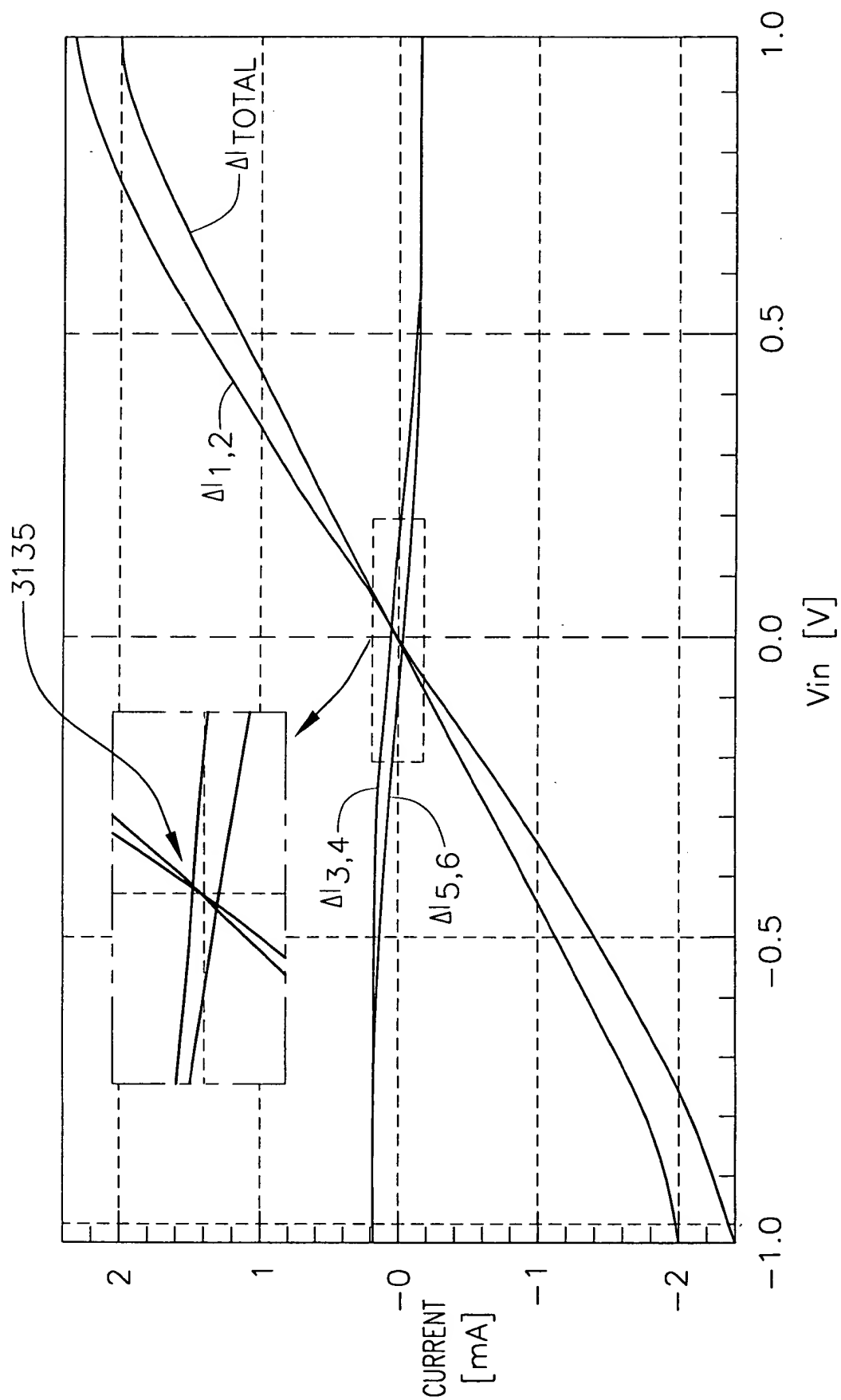
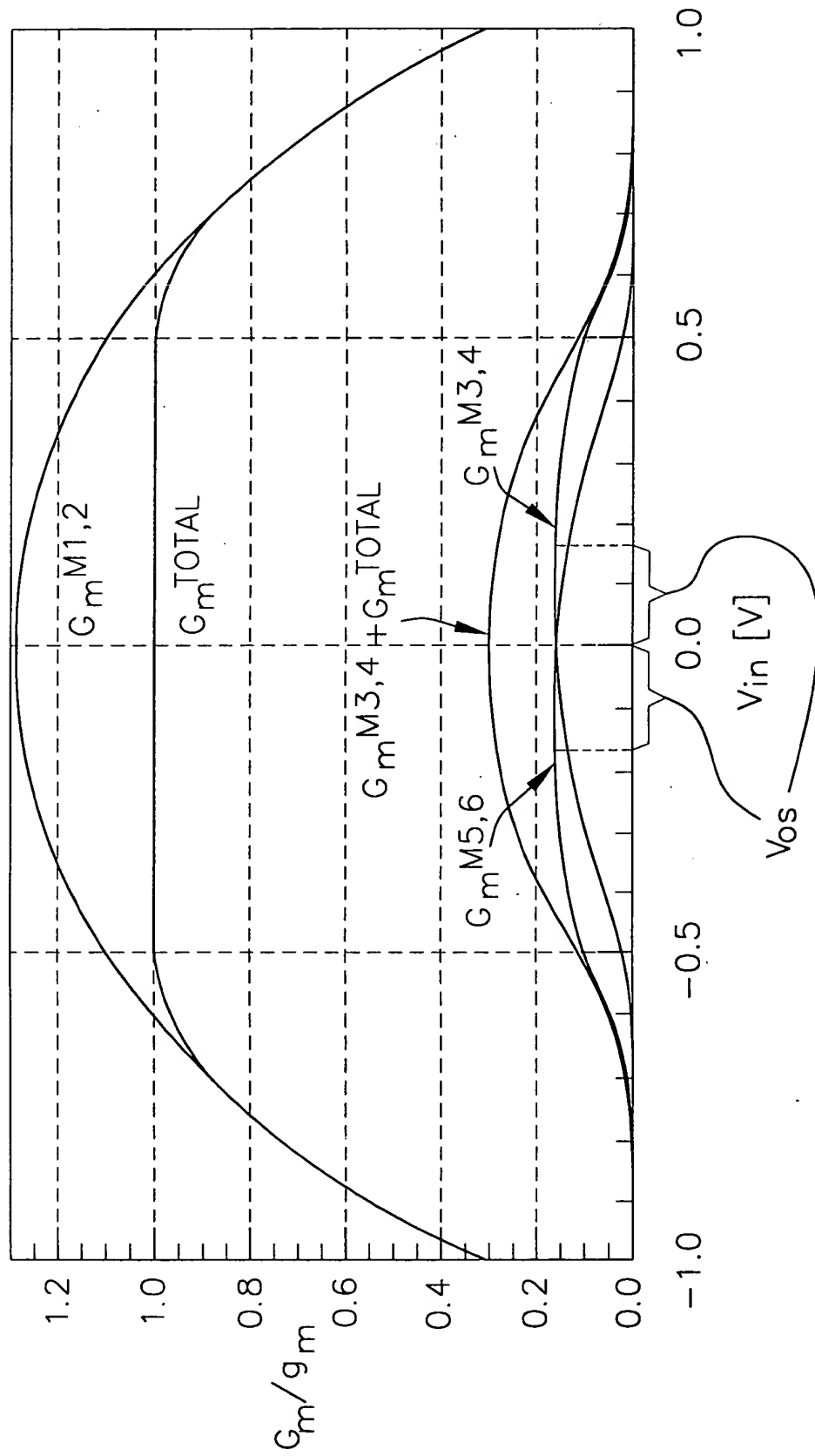




FIG. 31k



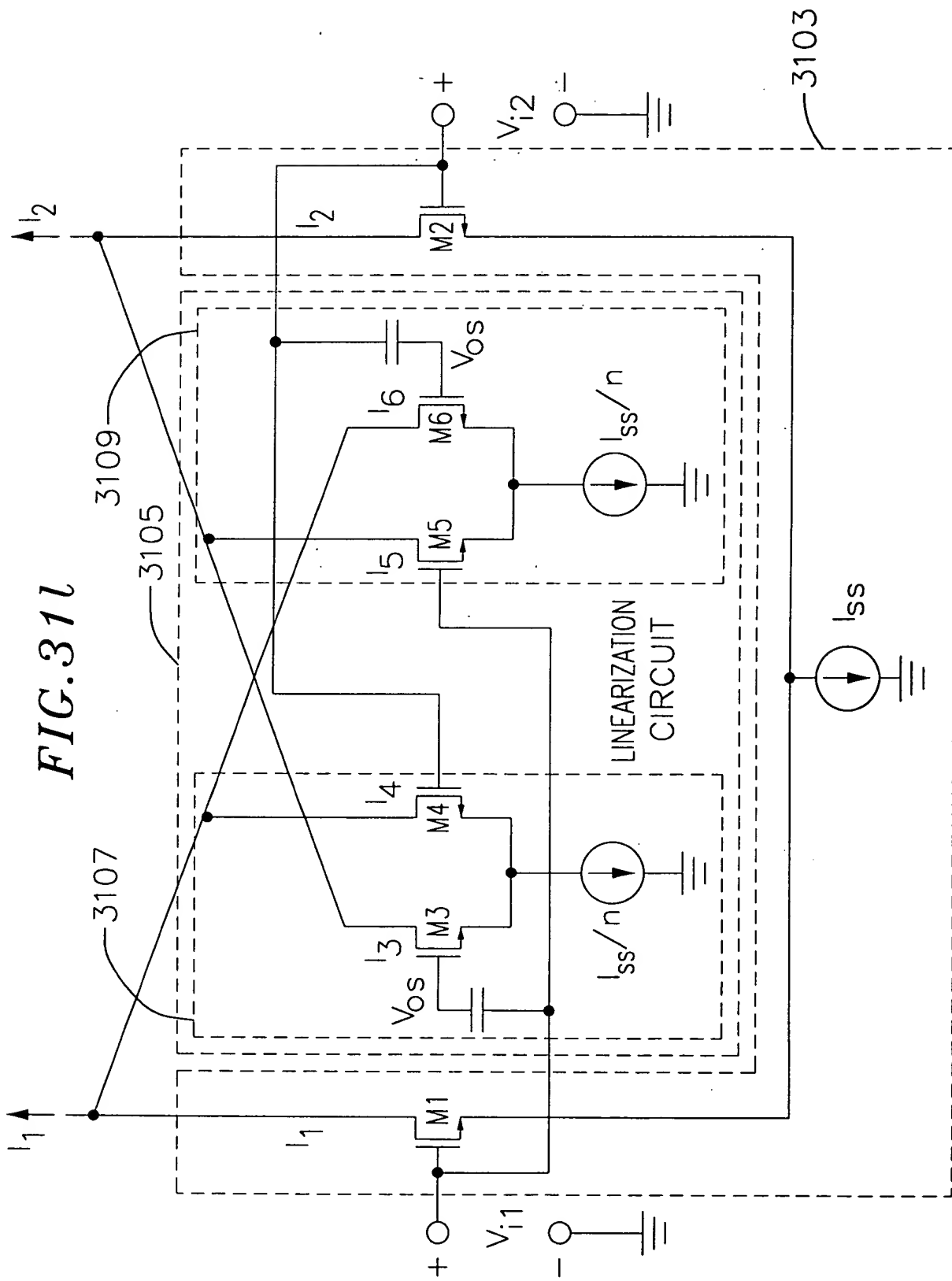


FIG. 31m

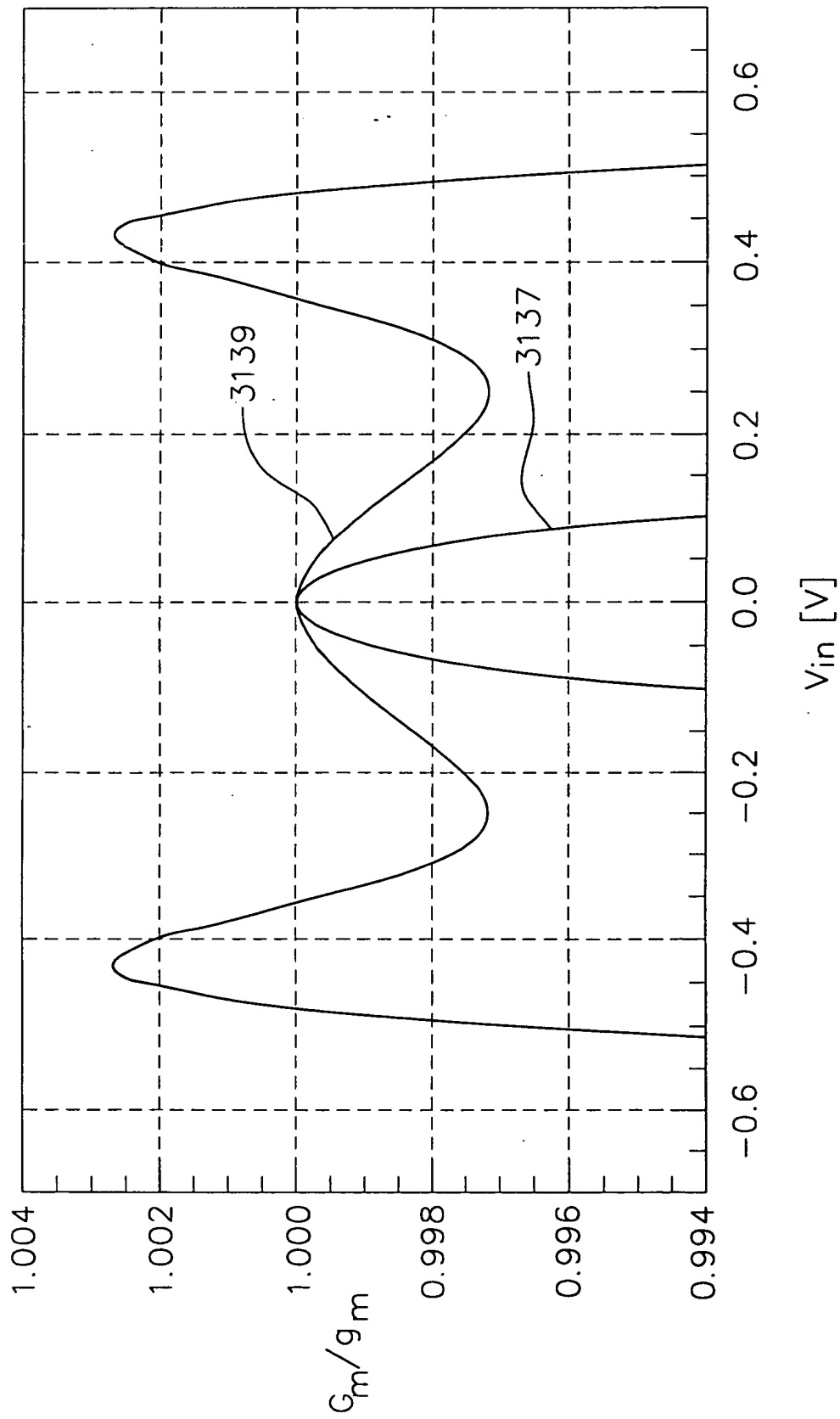


FIG. 32

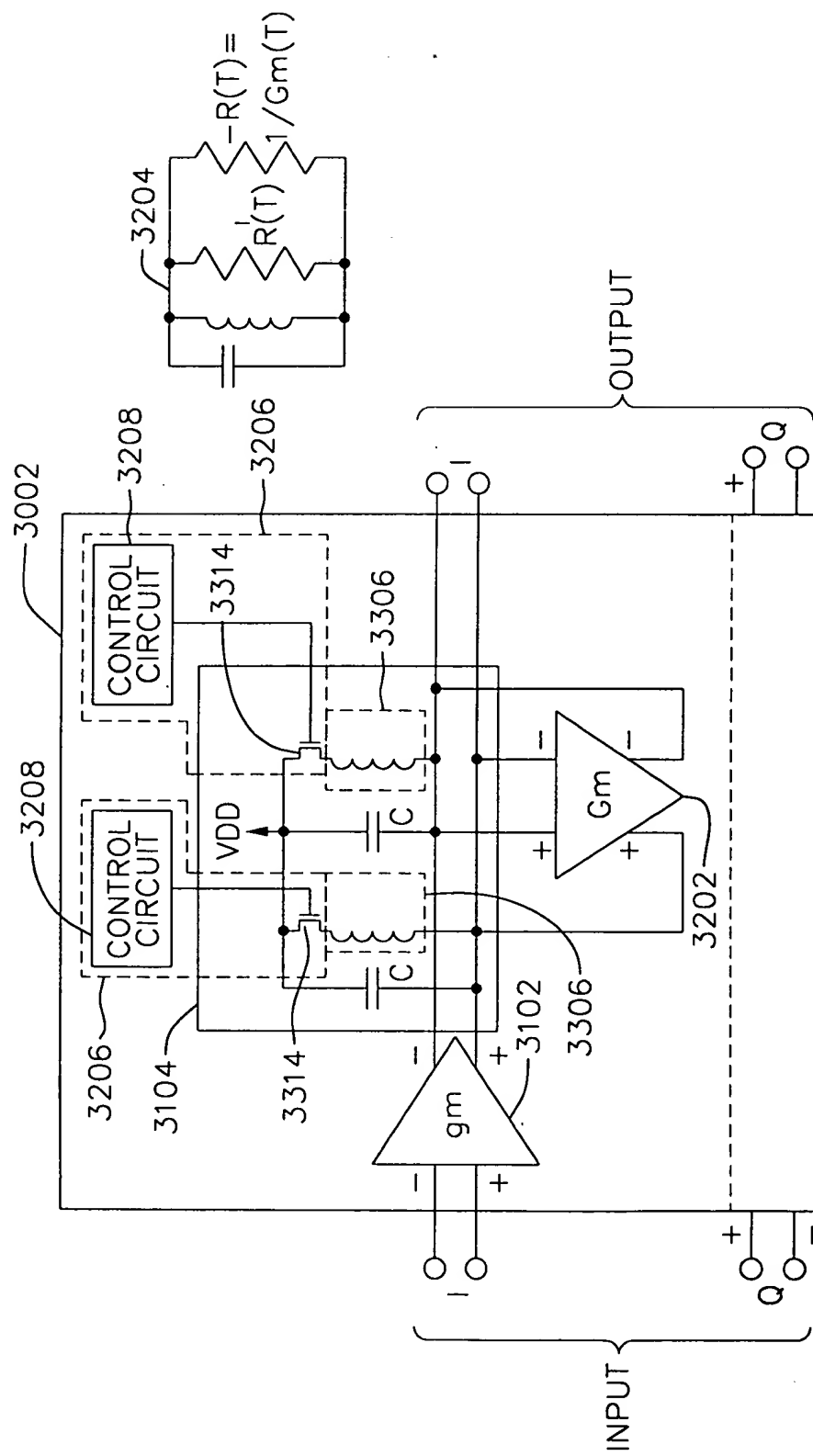


FIG. 33

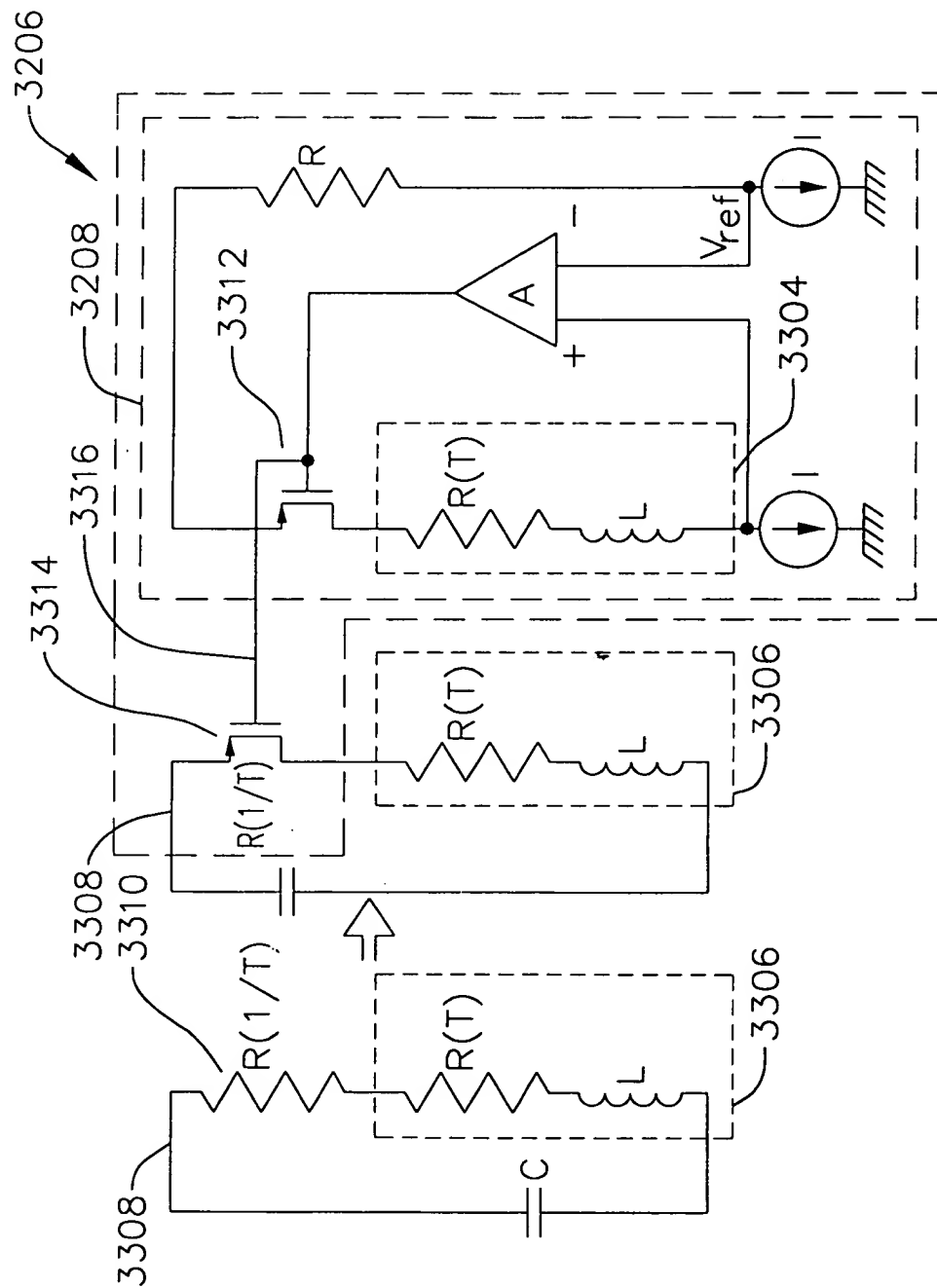
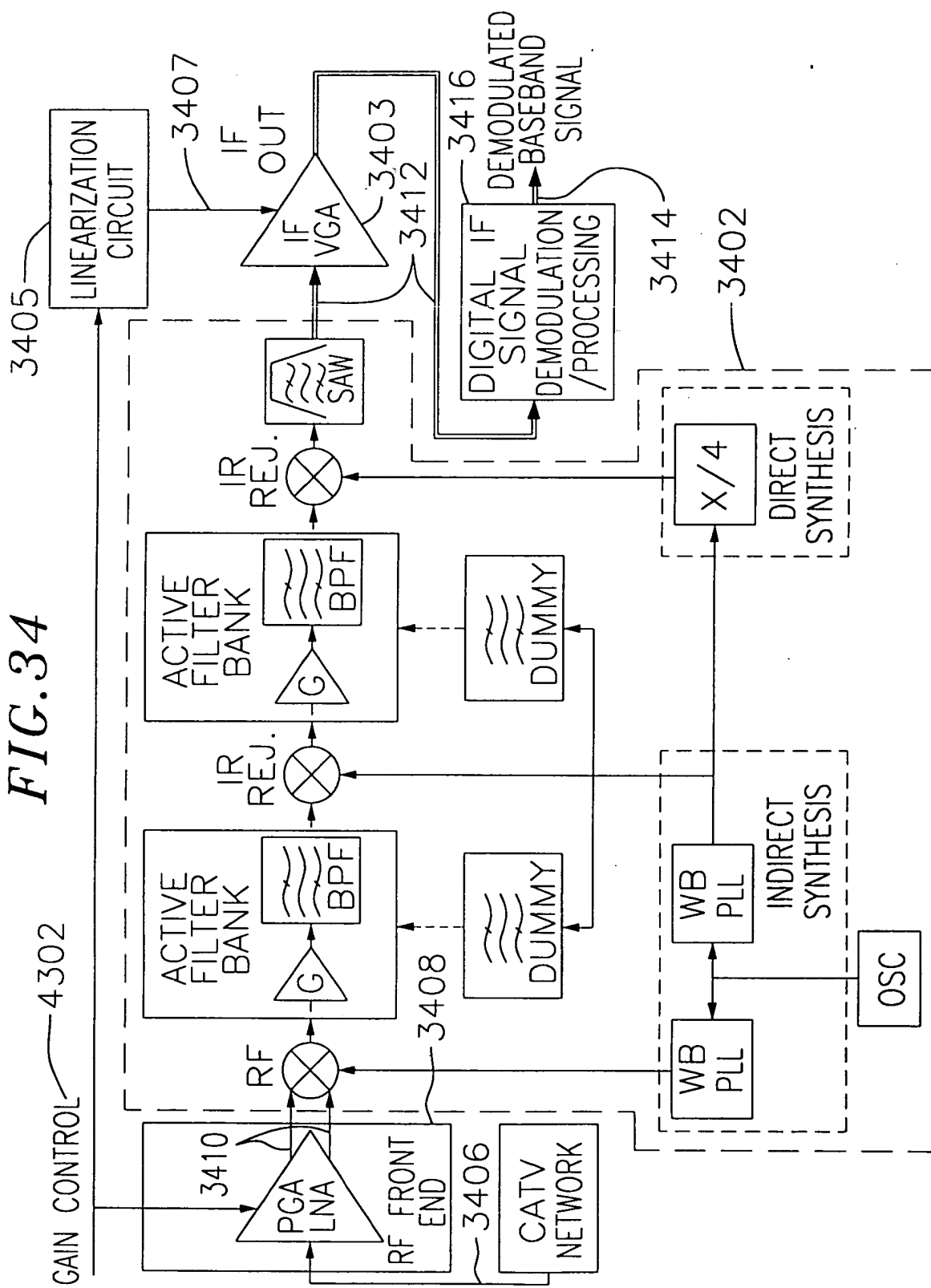


FIG. 34



*FIG.35*

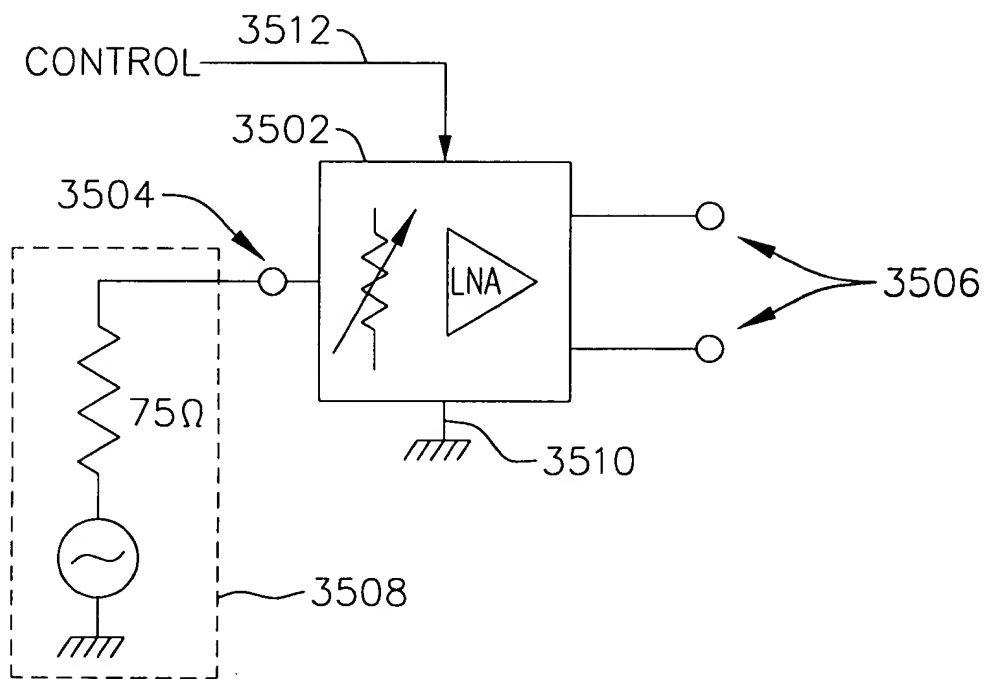






FIG. 37

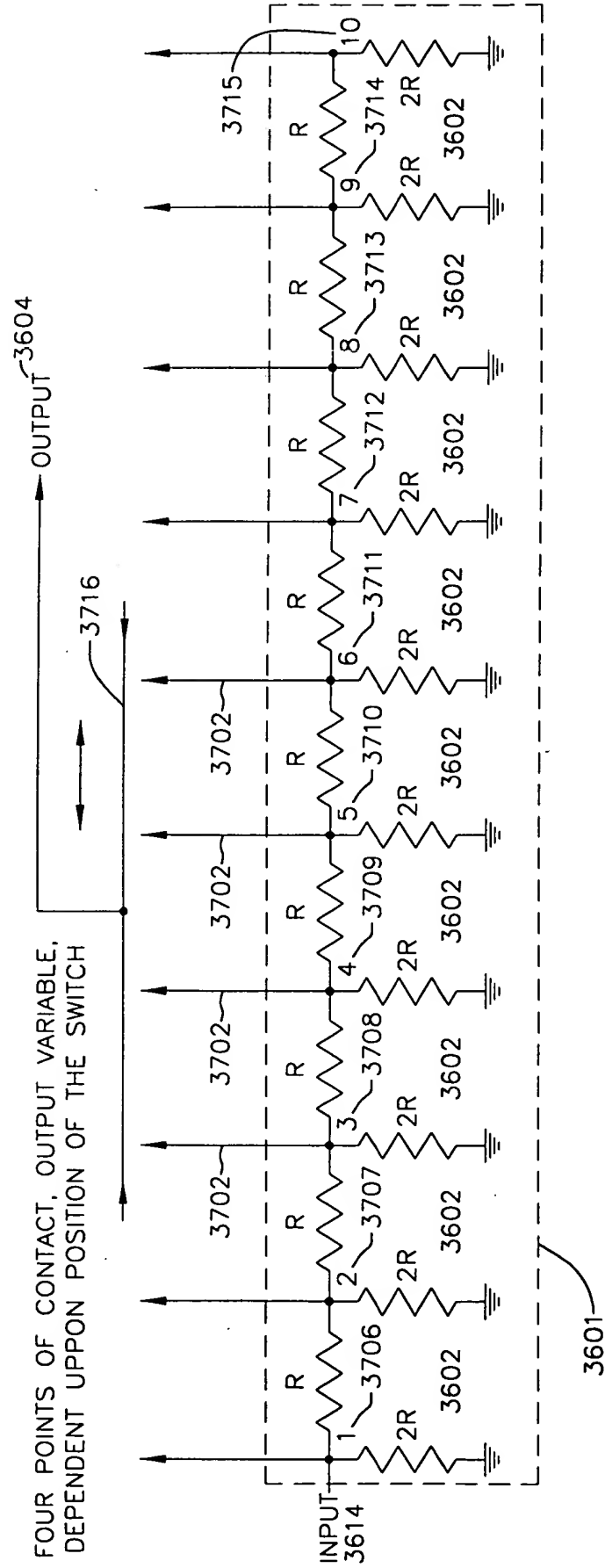


FIG.38

PGA SETTINGS

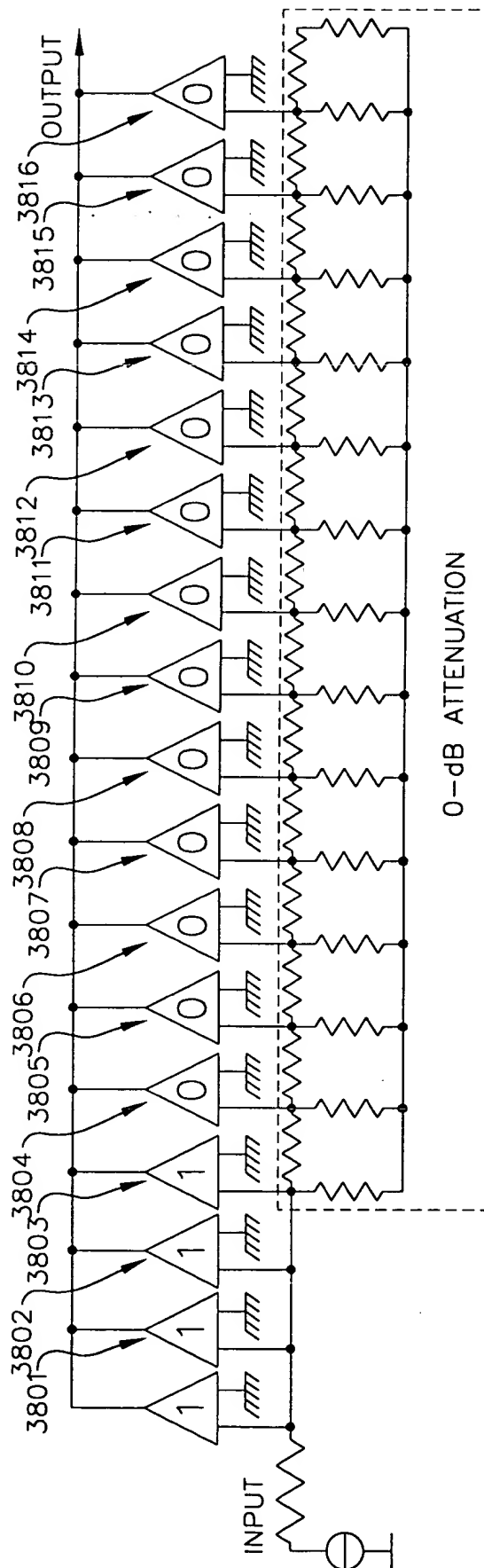


FIG. 39

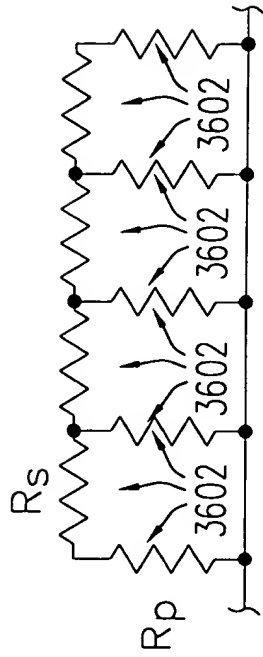


FIG. 40

PGA ARCHITECTURE

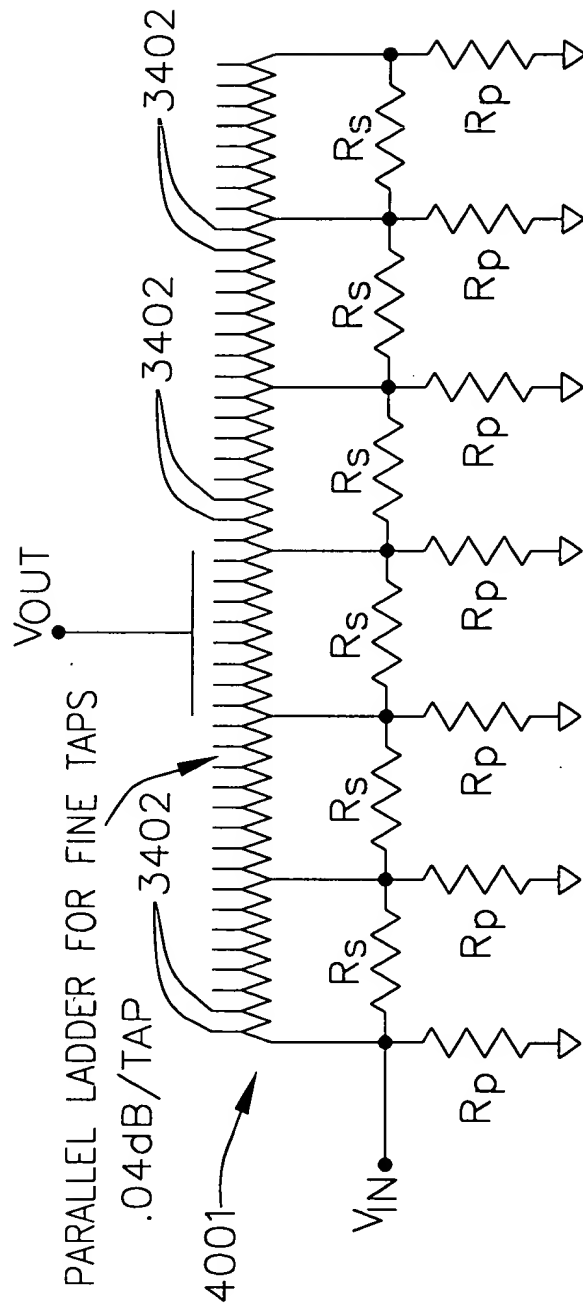


FIG. 41

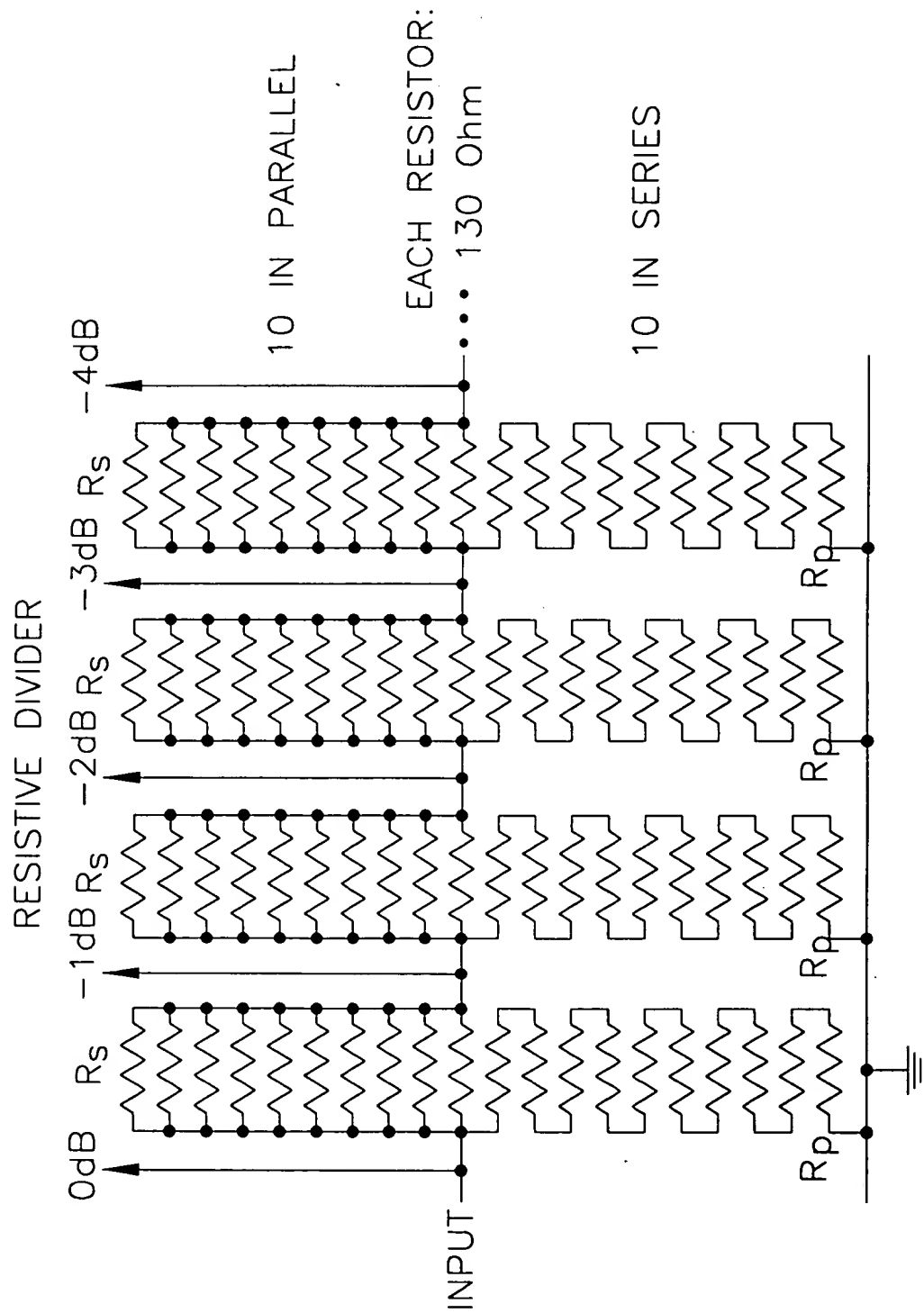
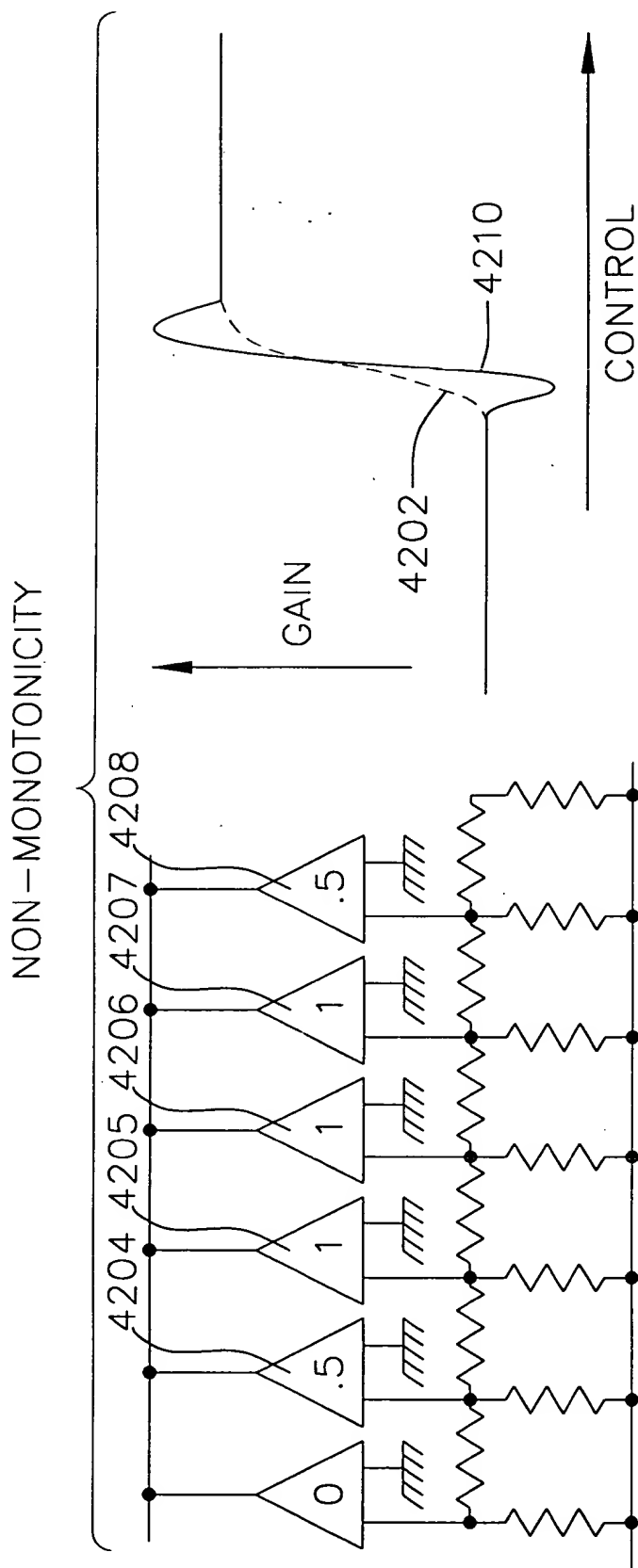
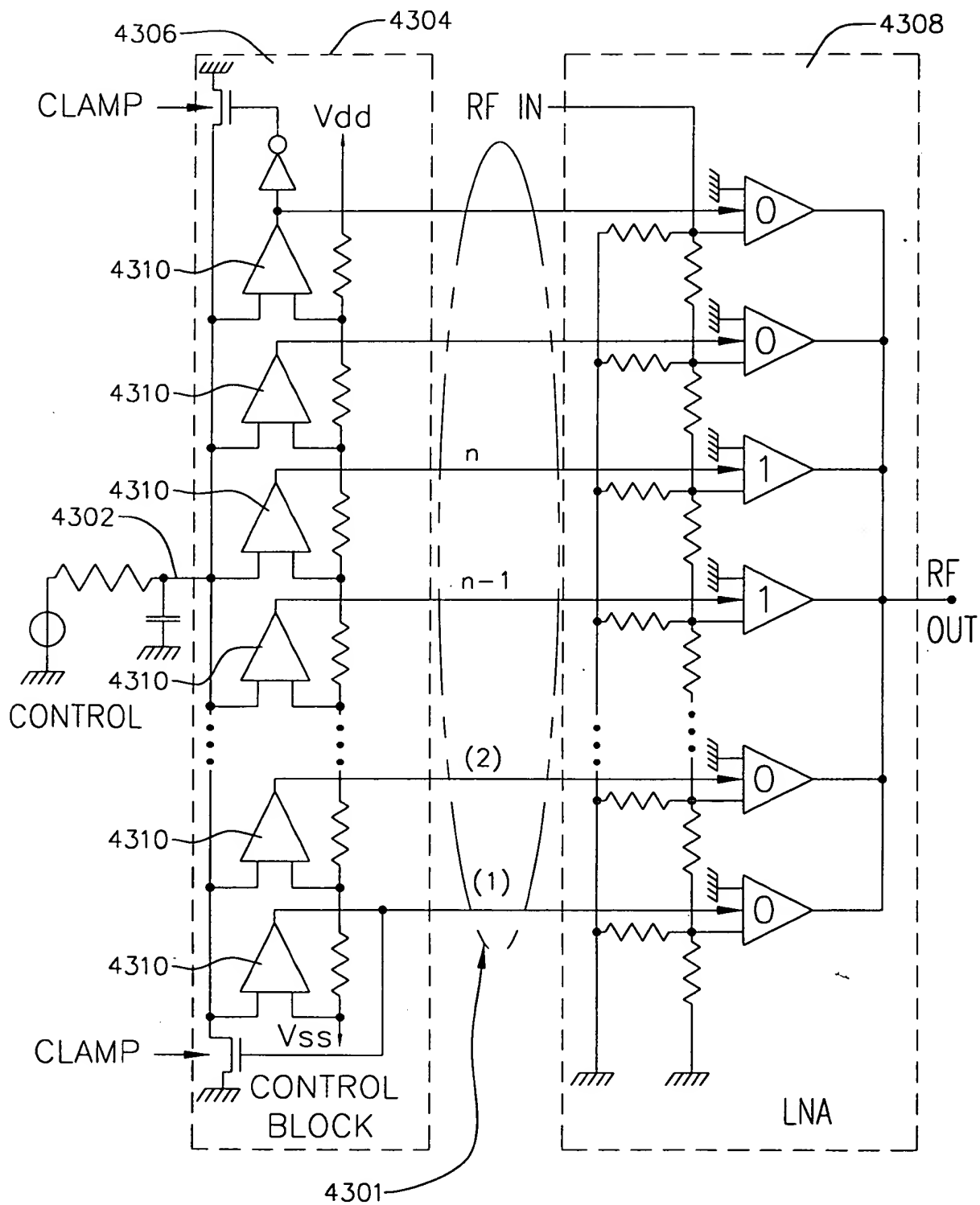


FIG. 42



## CLAMPING CONTROL RANGE



**FIG. 44a**  
CONTROLLED GAIN COMPARATOR

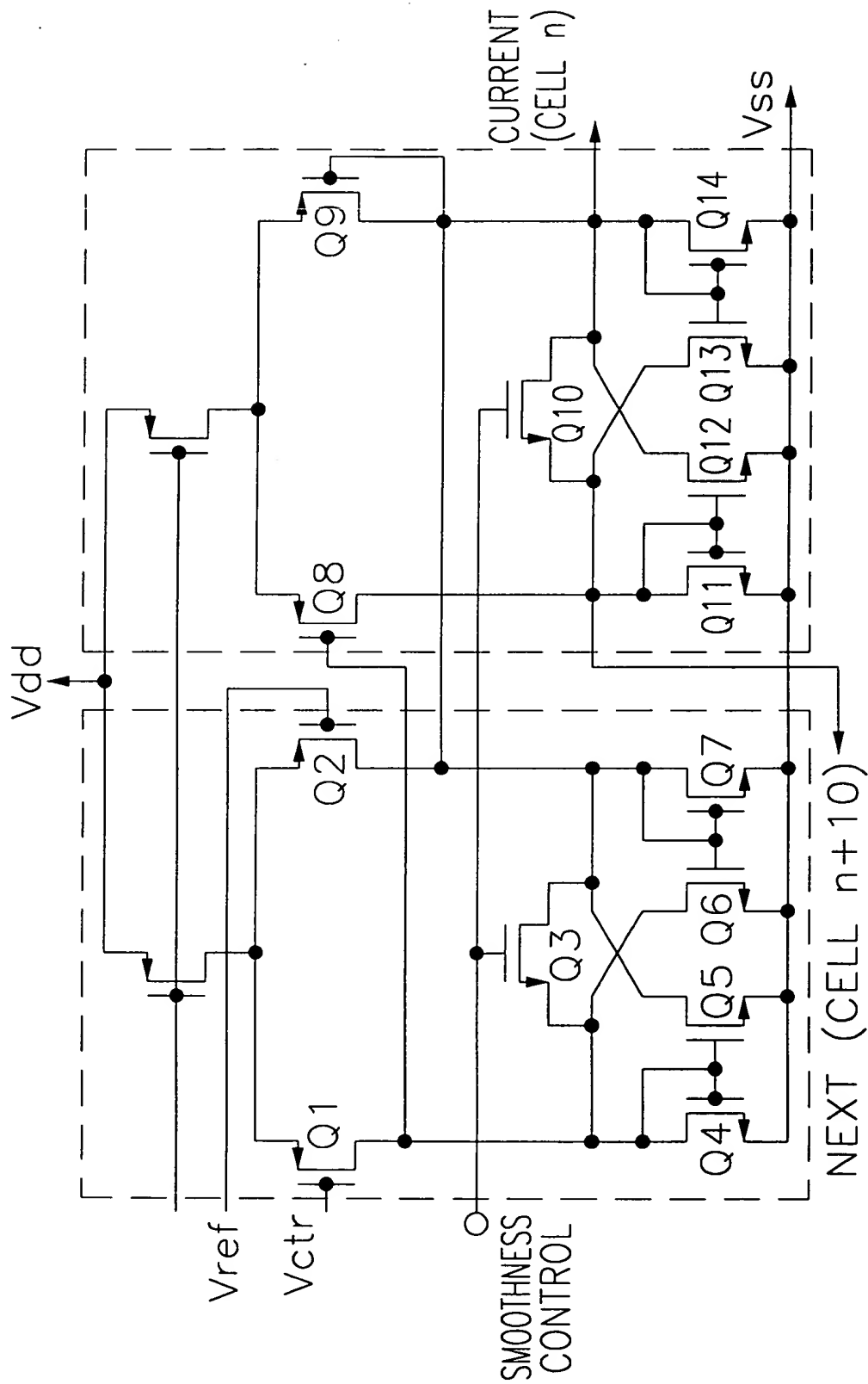


FIG. 44b

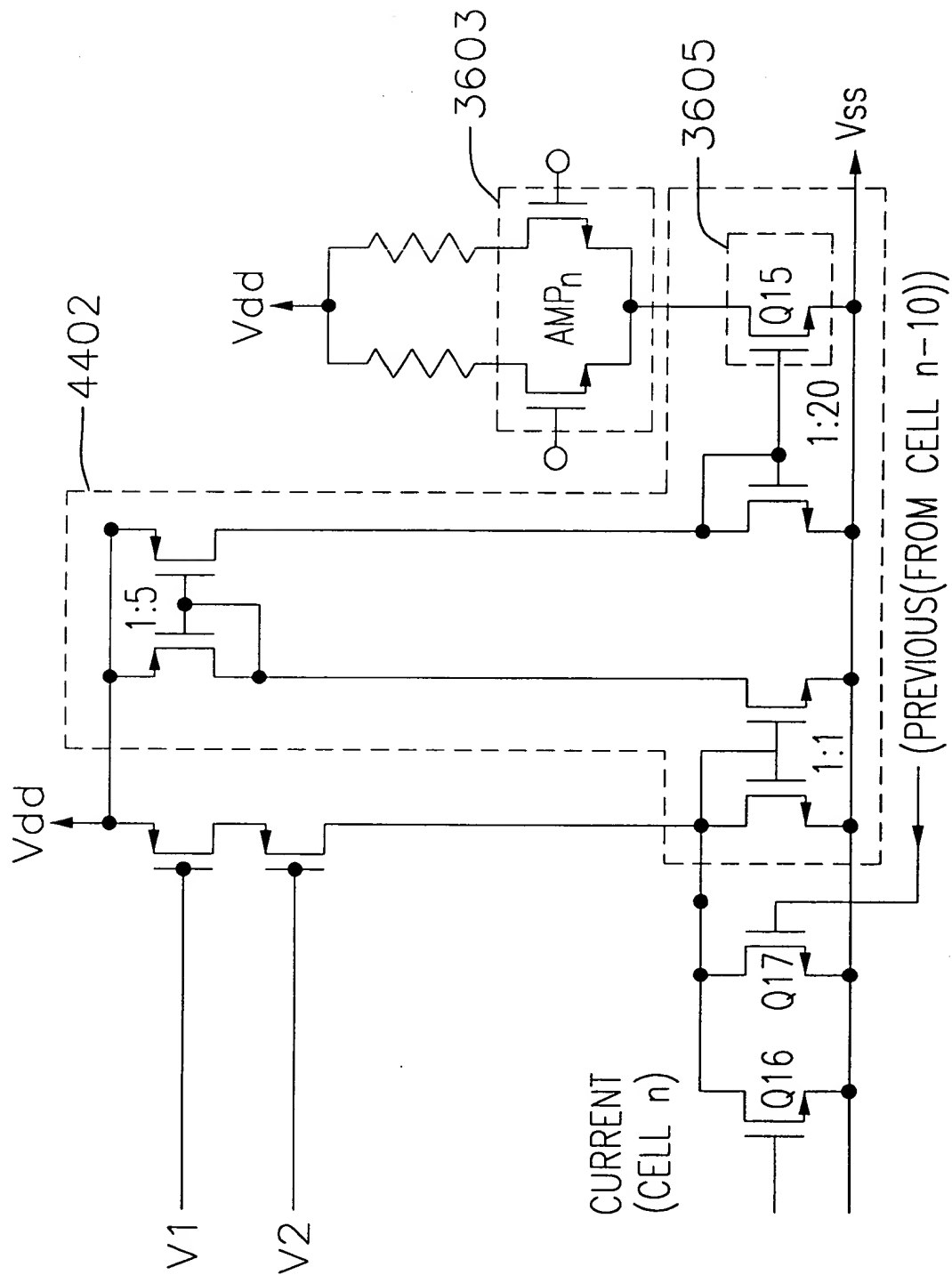
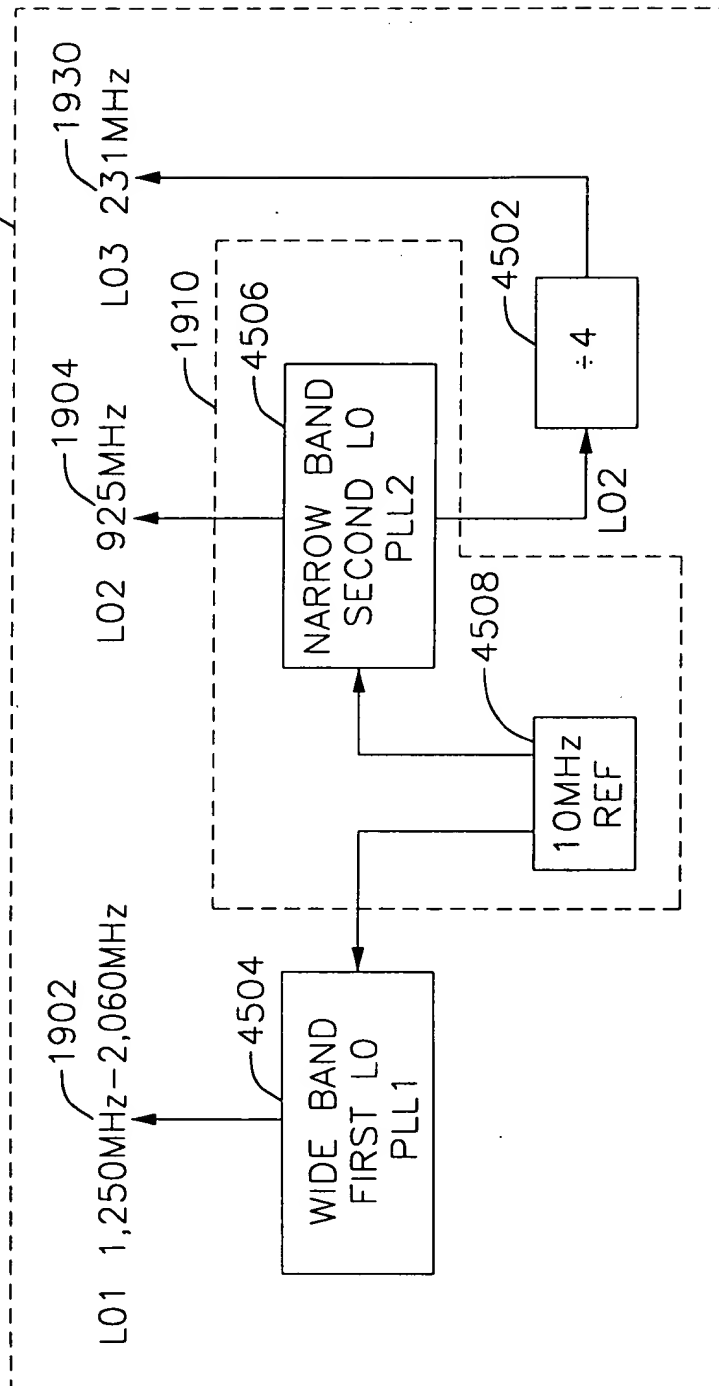




FIG. 45a



**FIG. 45b**

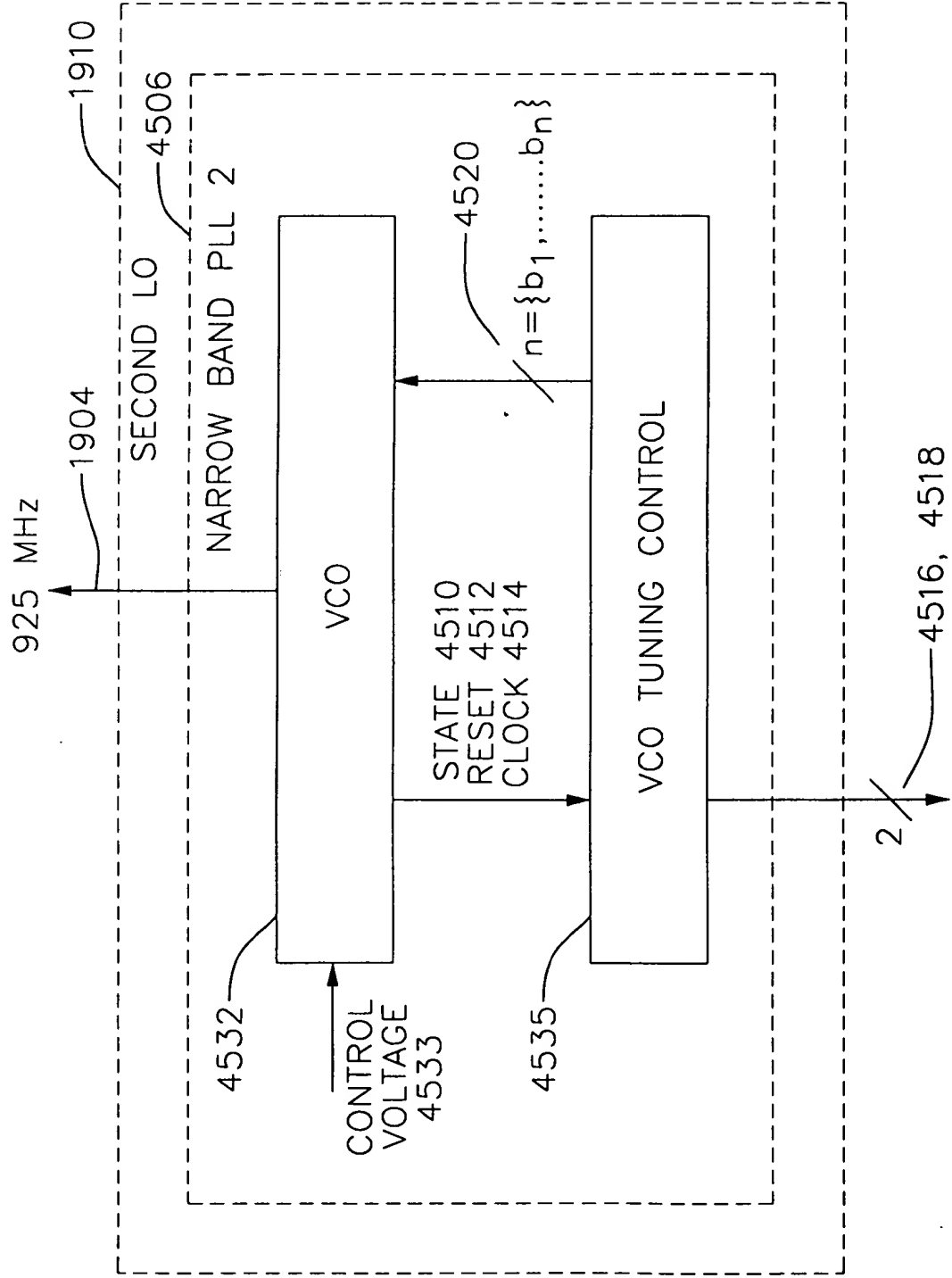


FIG. 45c

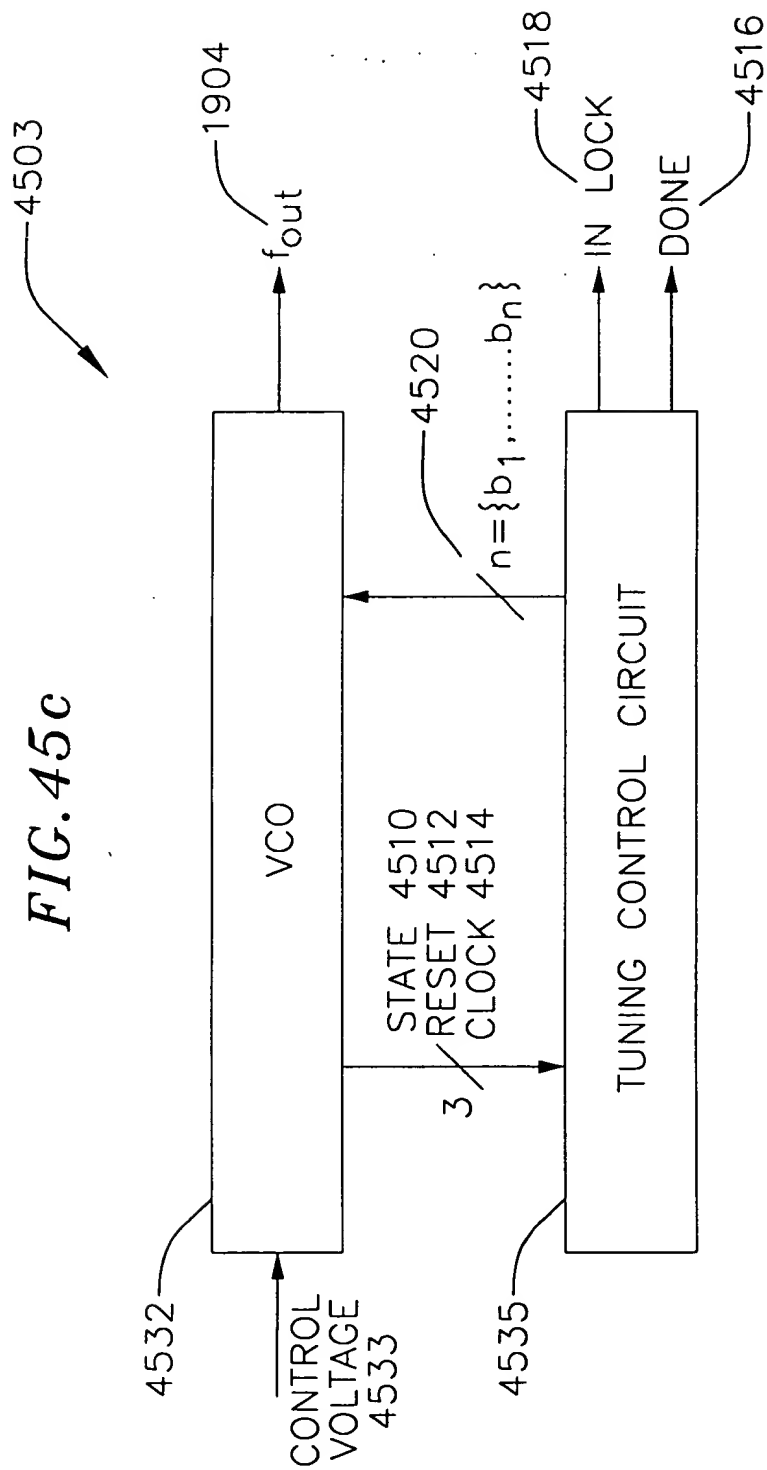
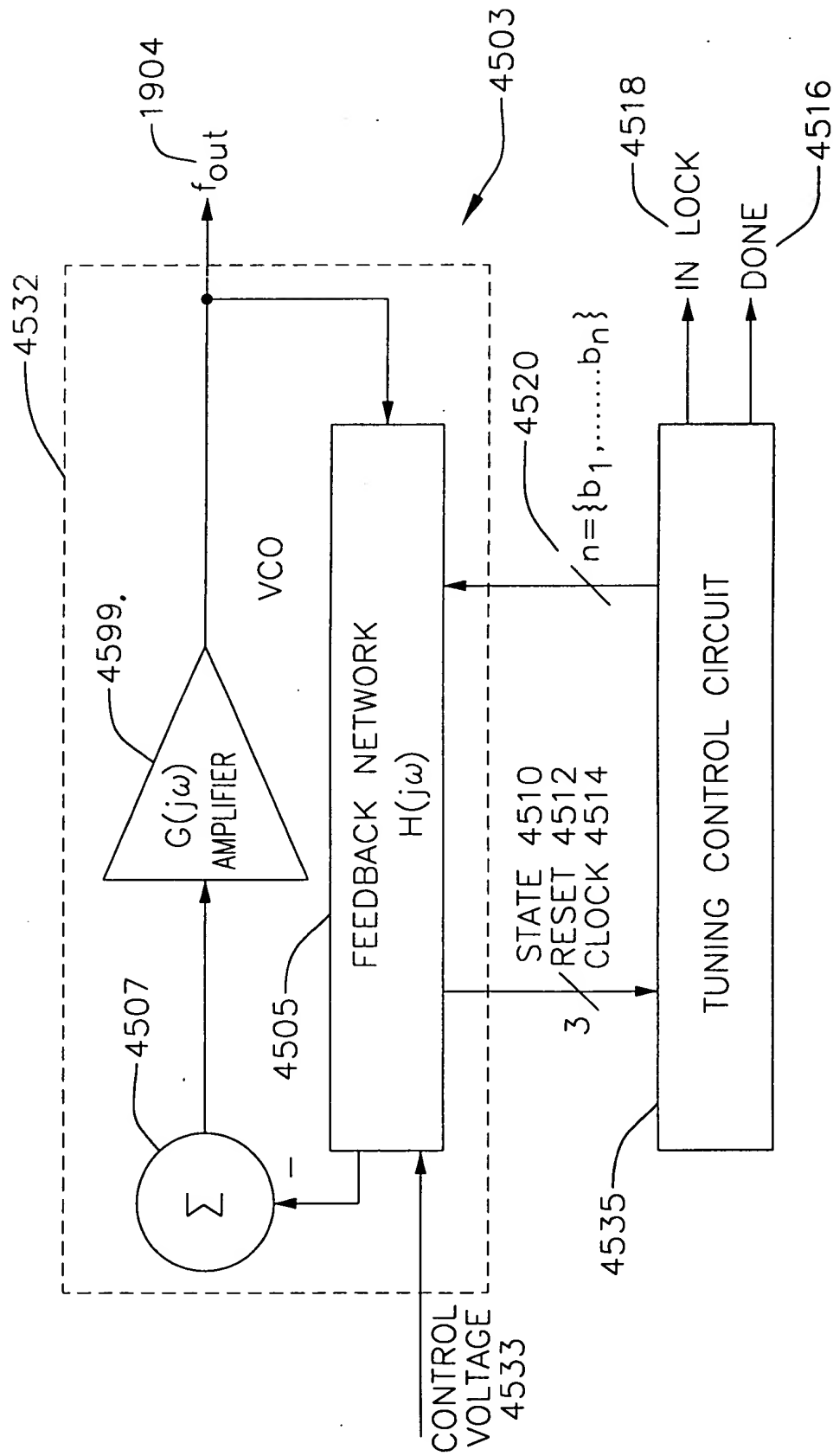


FIG. 455d



**FIG. 45e**

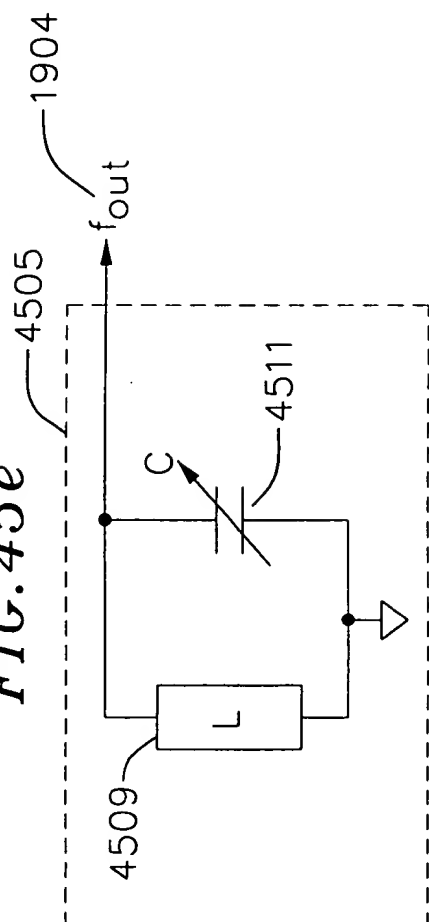
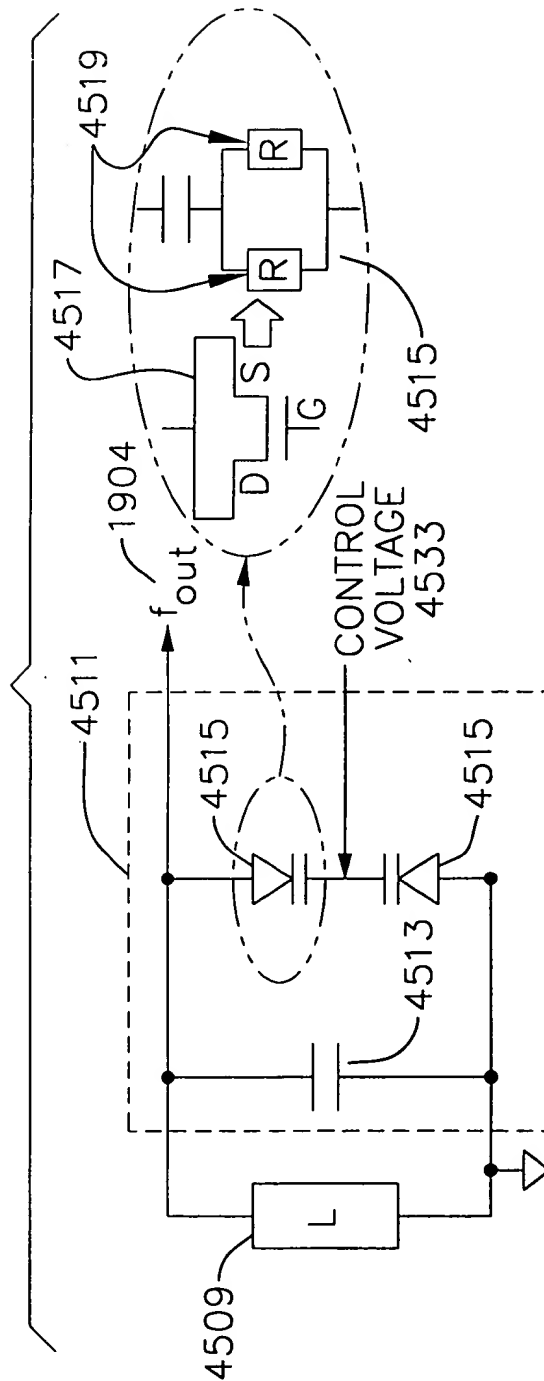


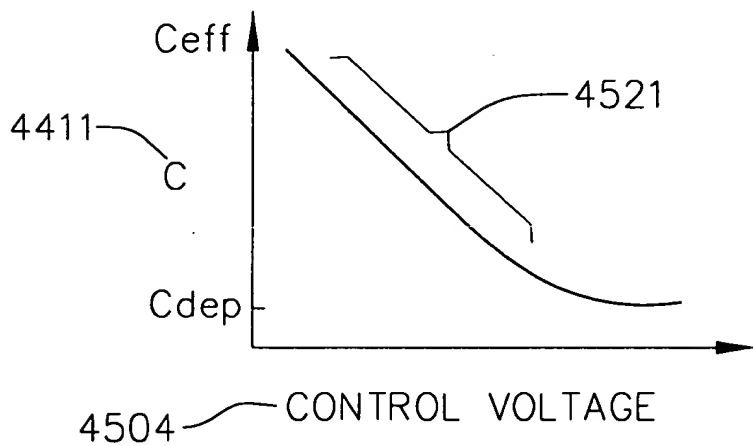
FIG. 45f



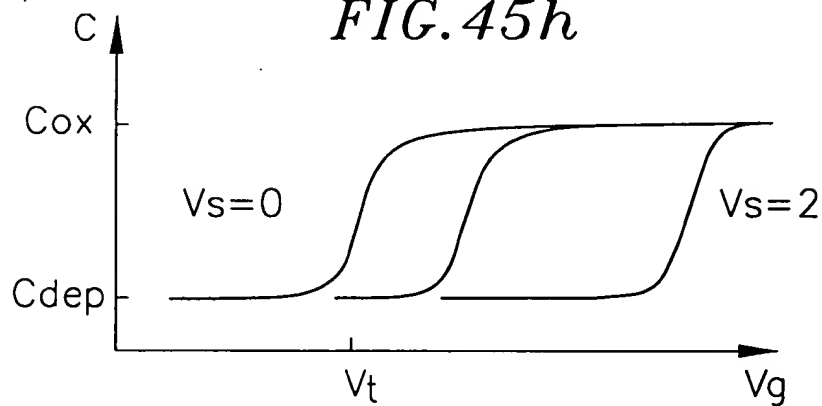


*FIG. 45g*

CAPACITANCE VS CONTROL VOLTAGE



*FIG. 45h*



*FIG. 45j*

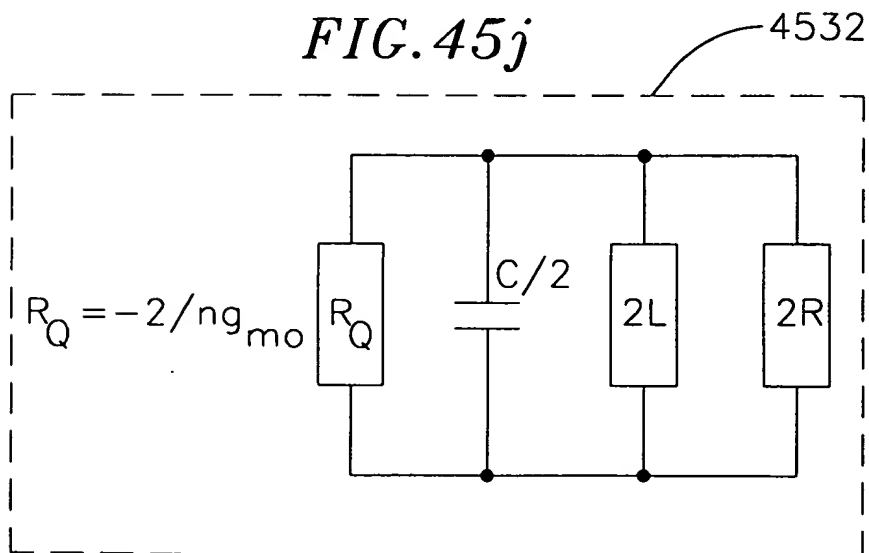


FIG. 45i

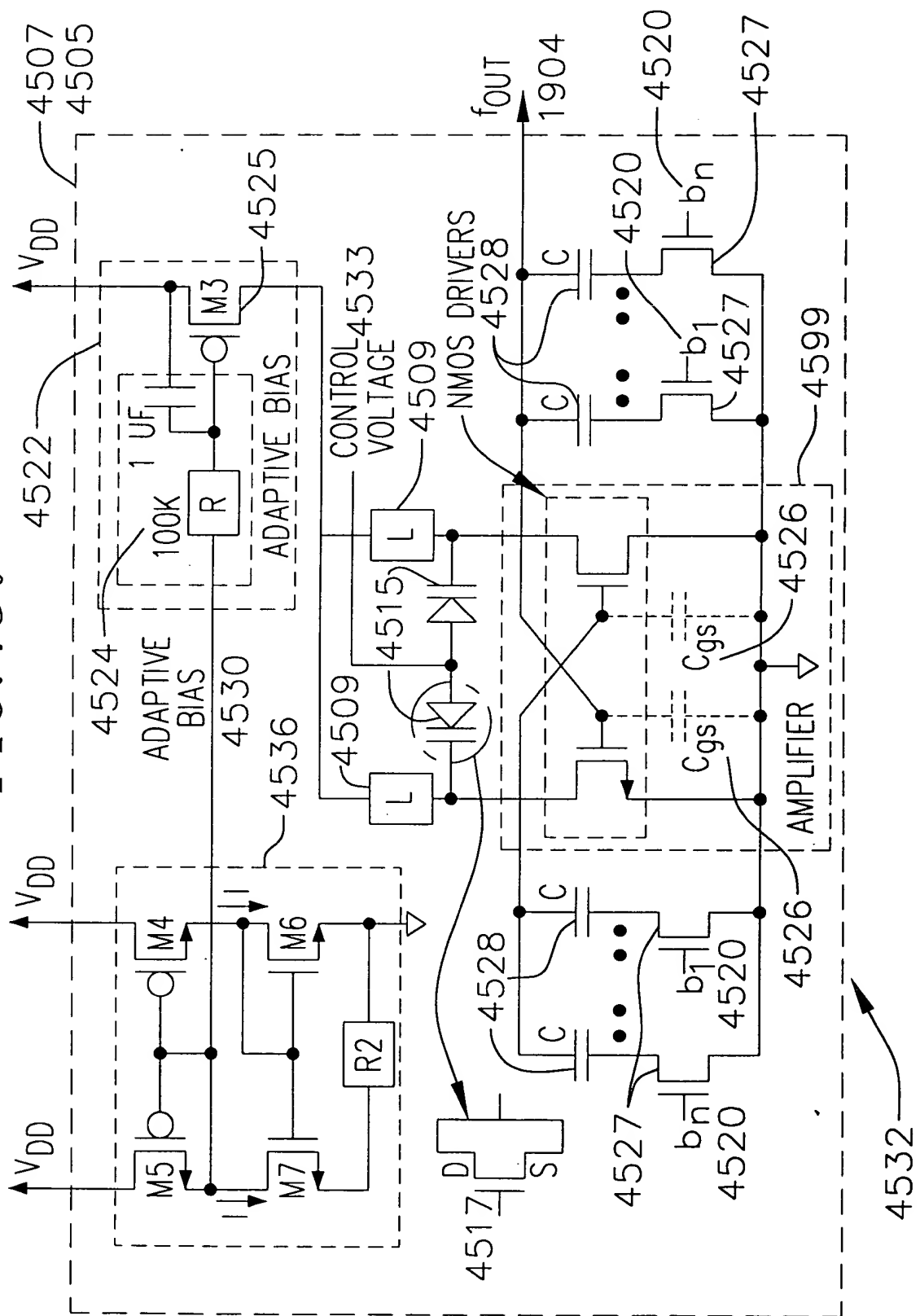
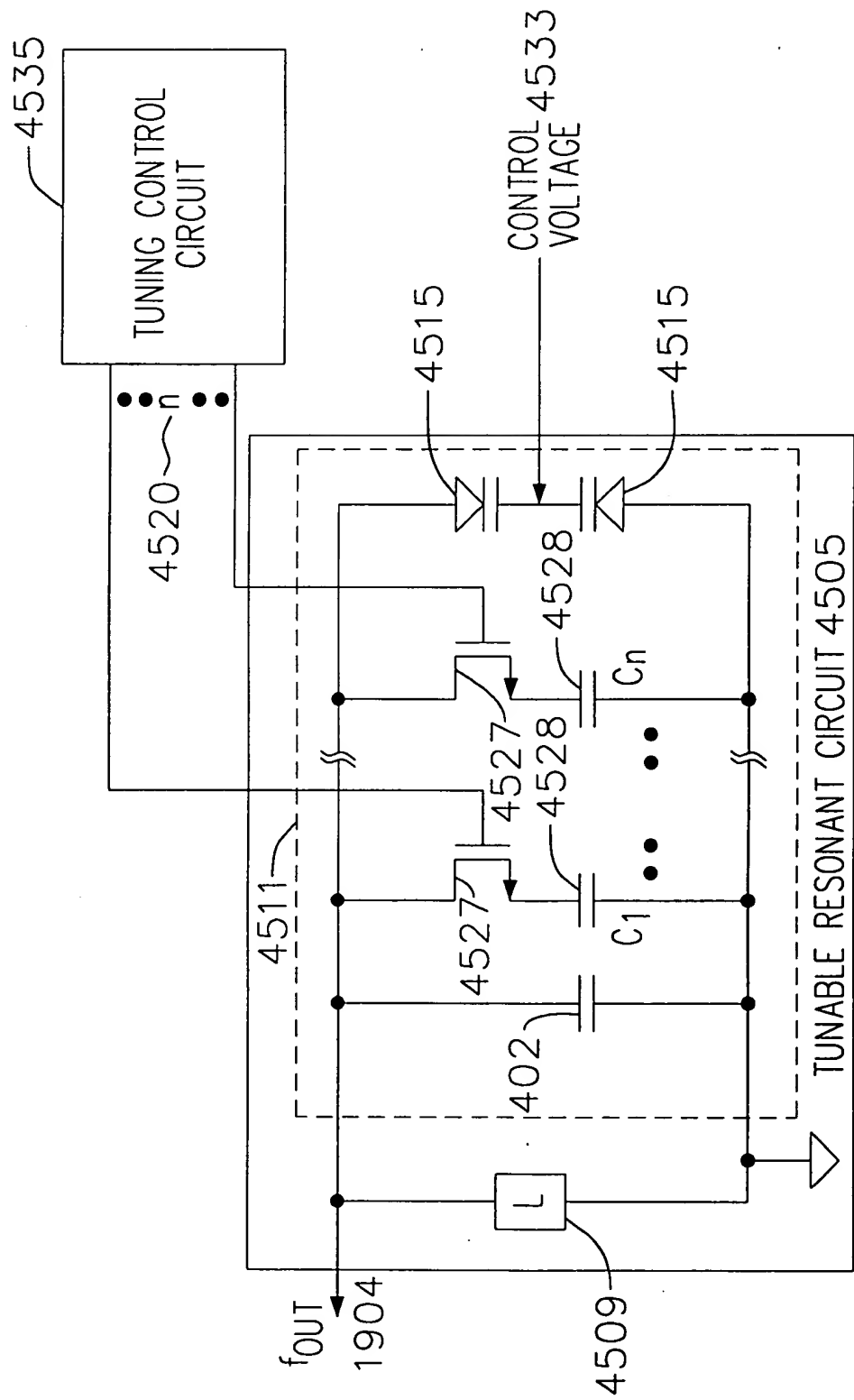
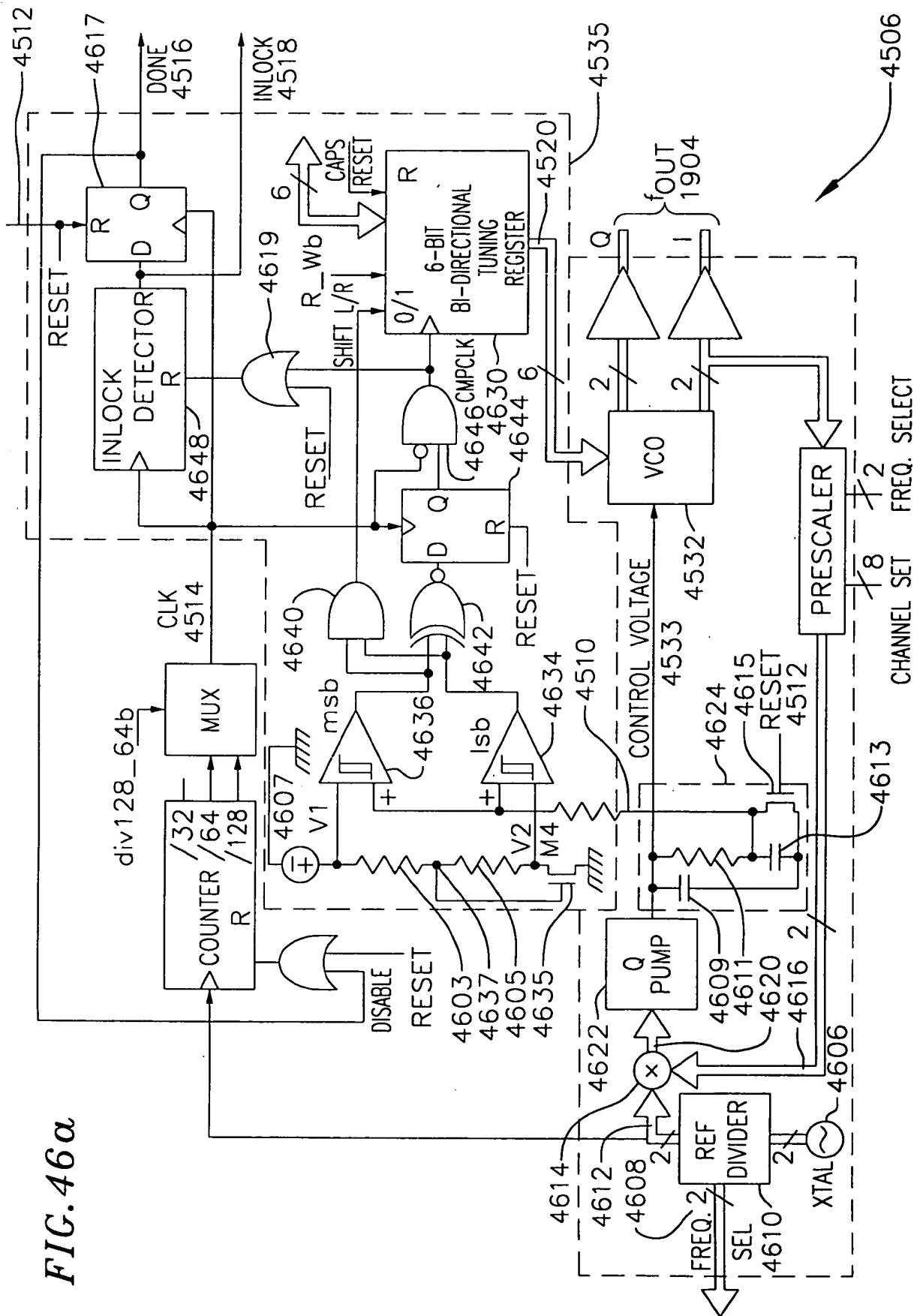


FIG. 45k







*FIG. 46b*

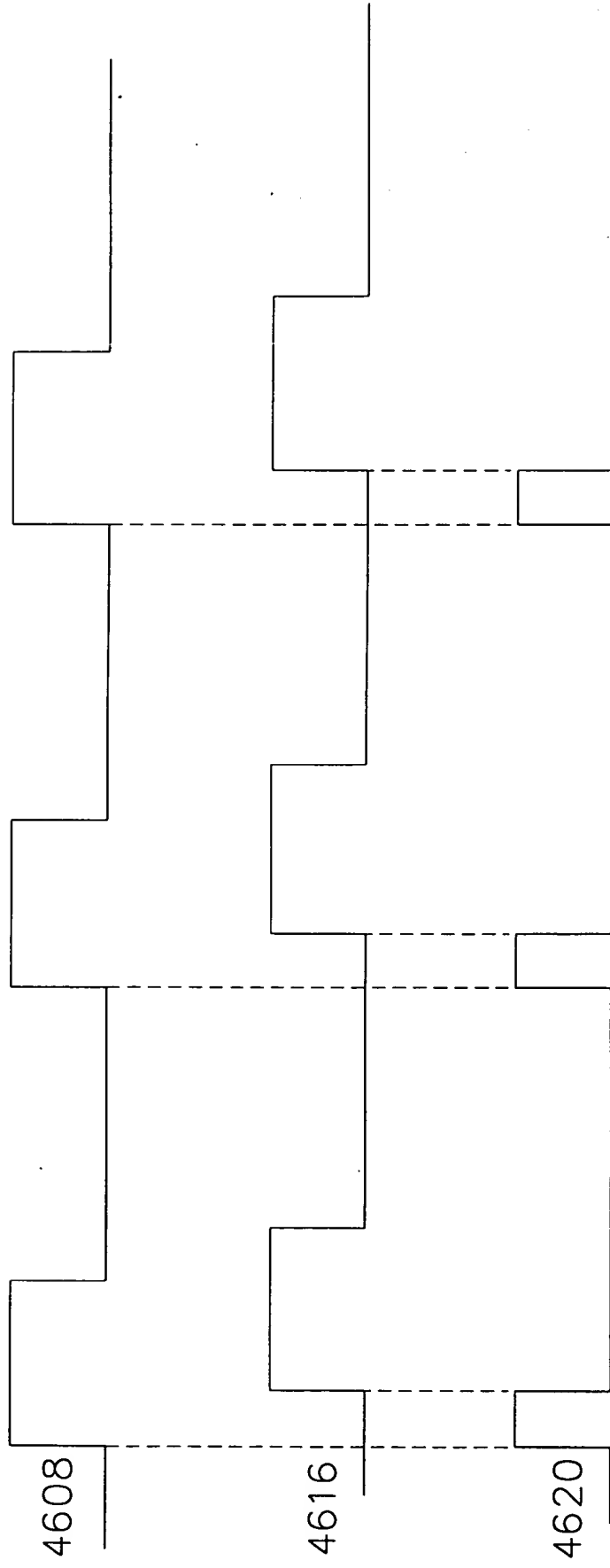


FIG. 47a

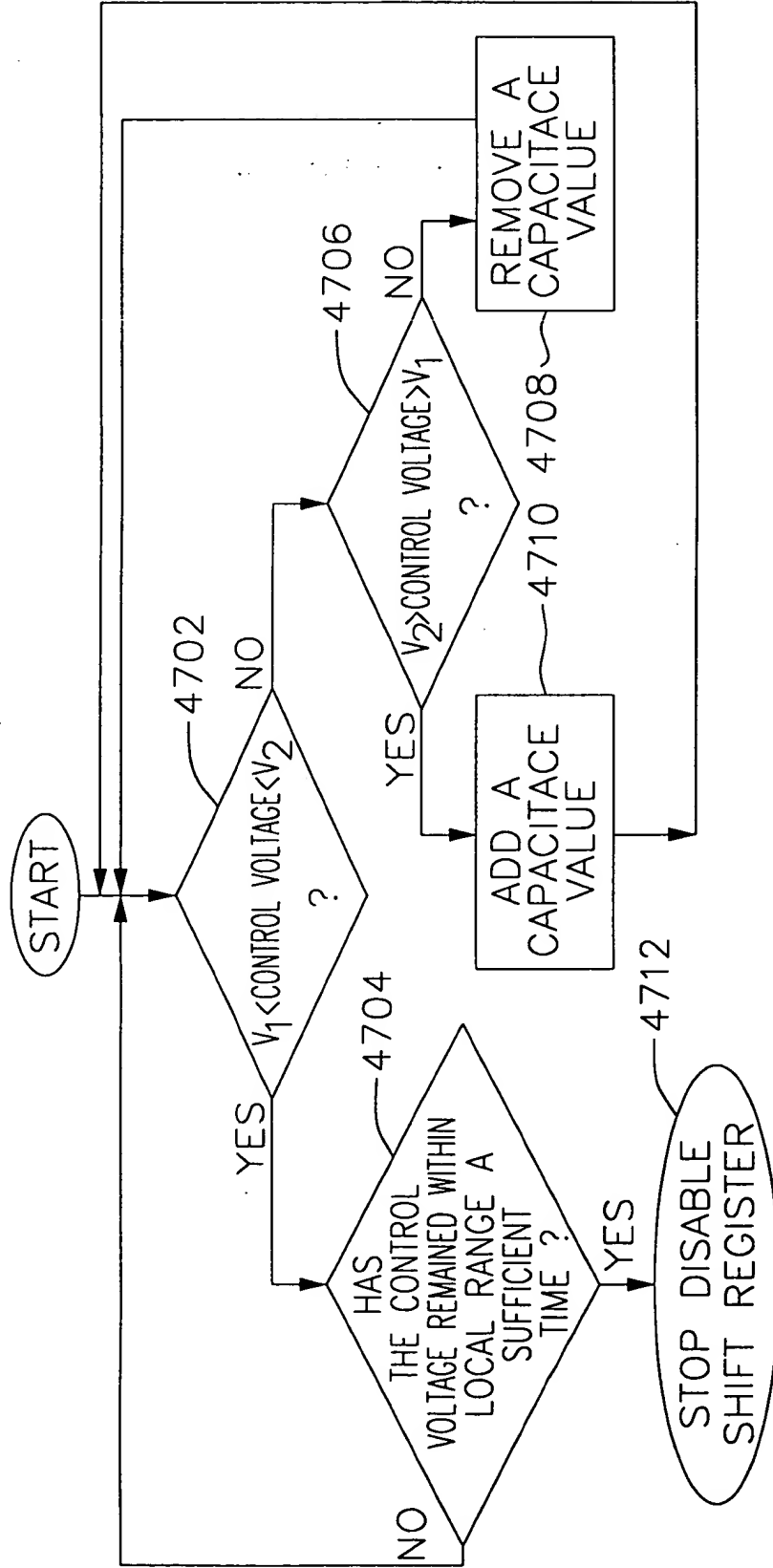


FIG. 47b

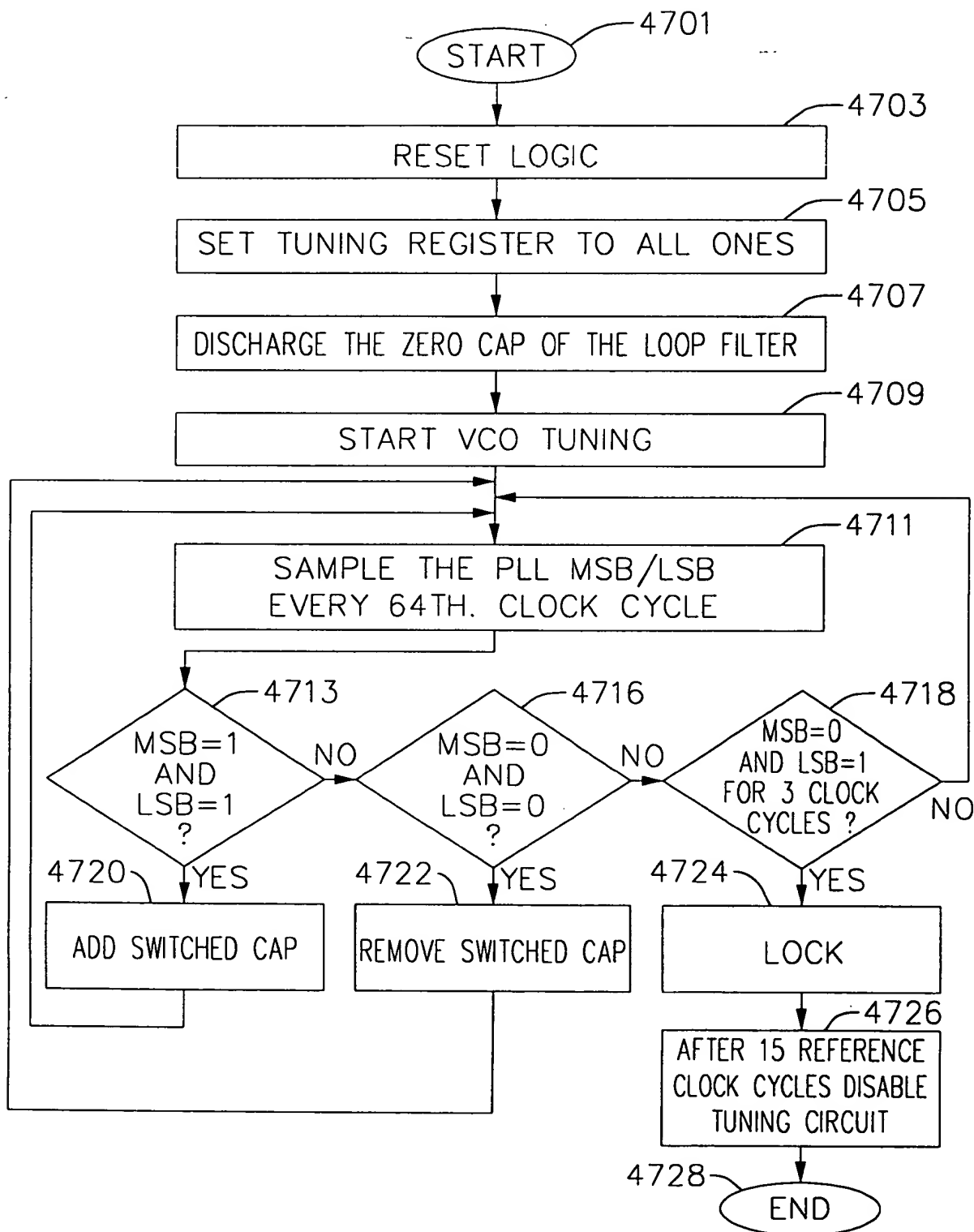


FIG. 47c

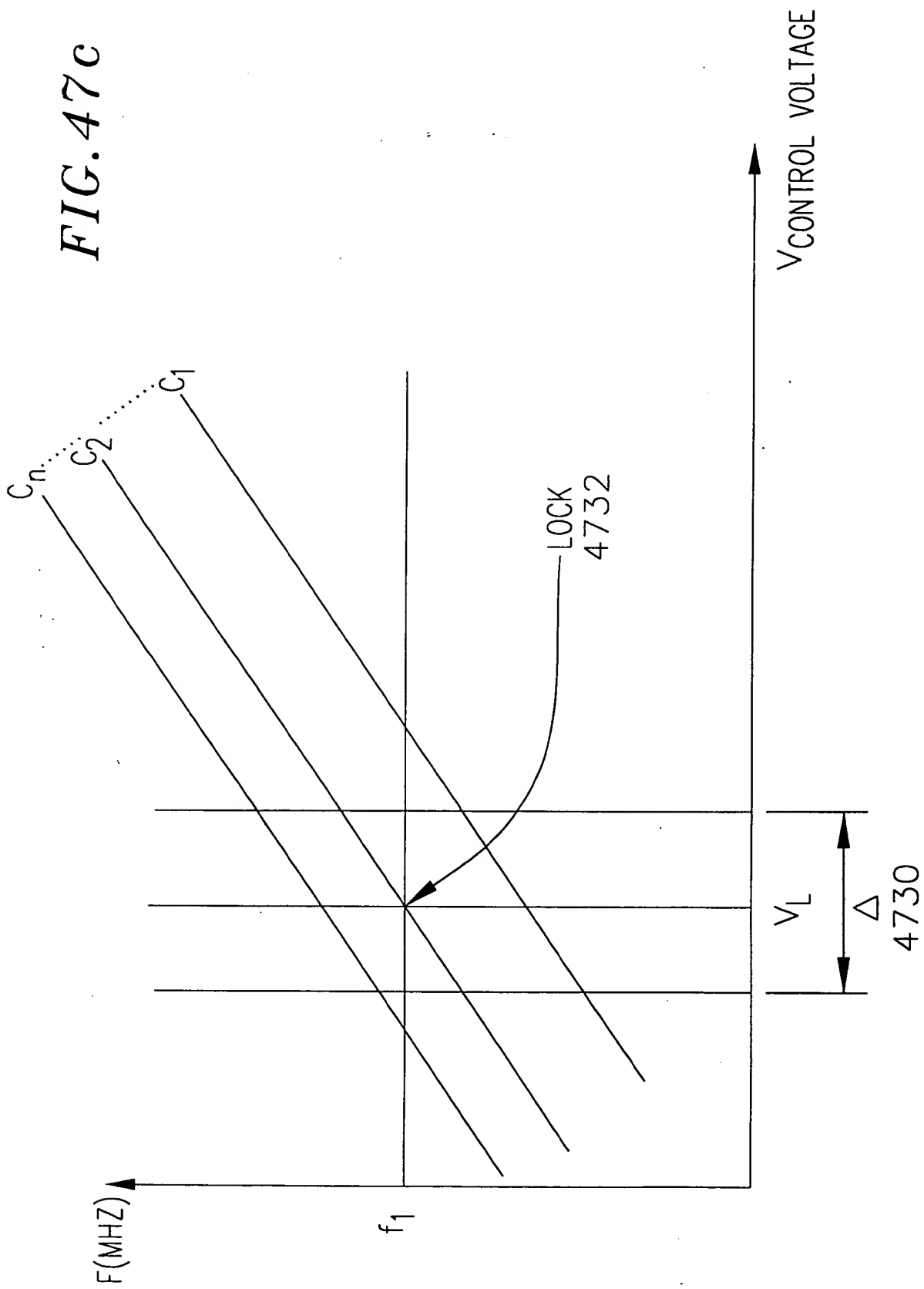


FIG. 47d

REPRESENTATIVE  $K_{VCO}$  CURVES

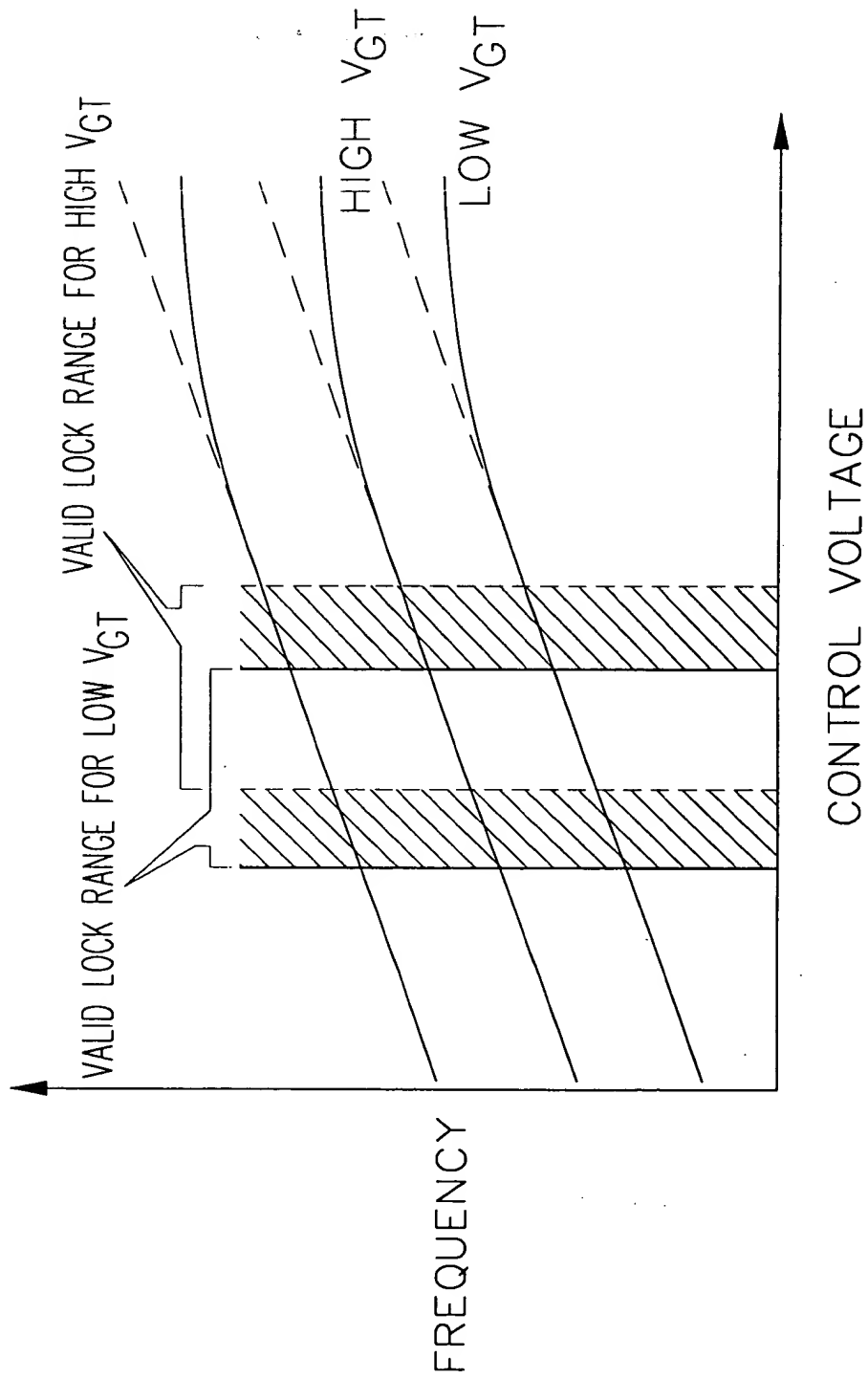




FIG. 49

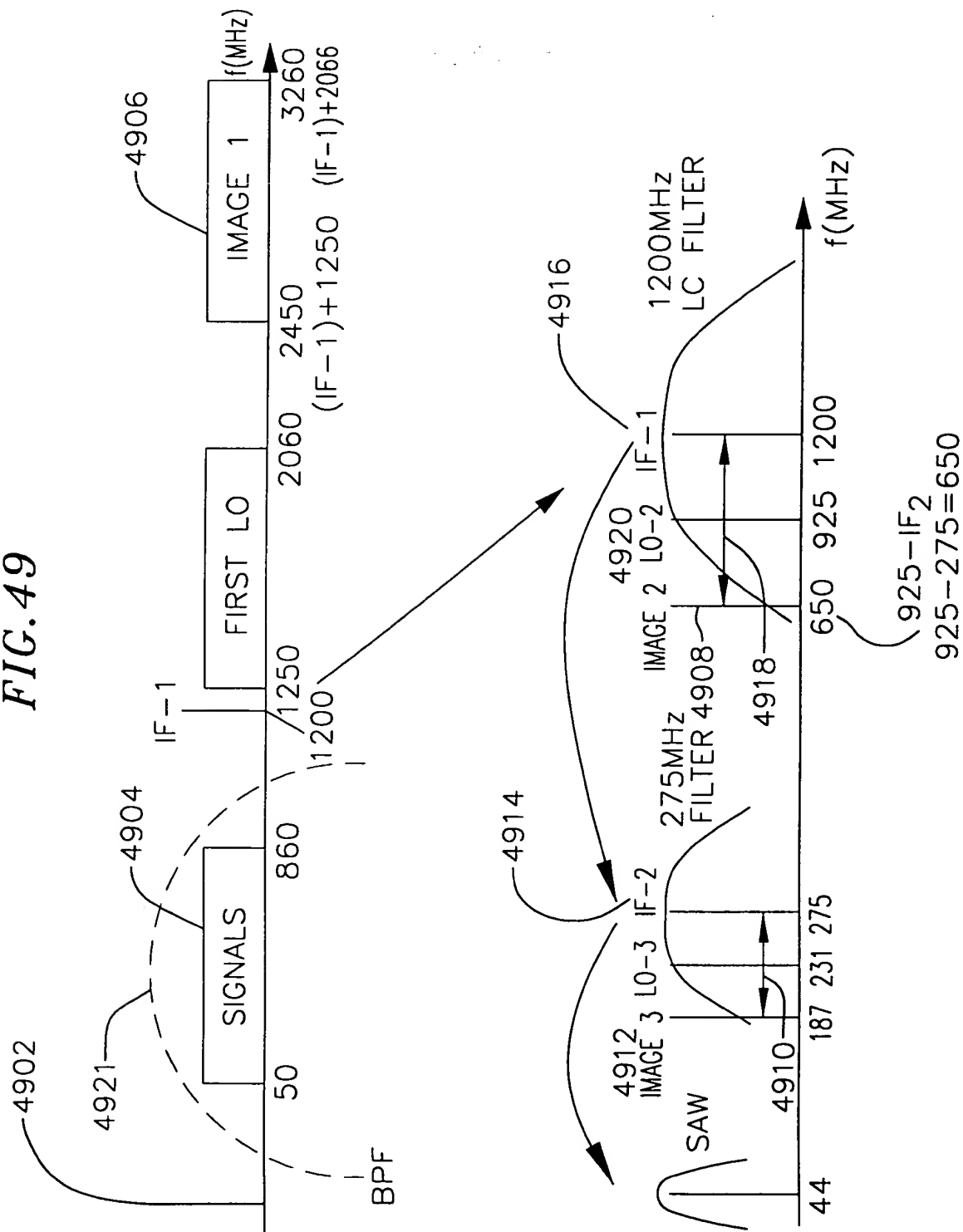




FIG. 50

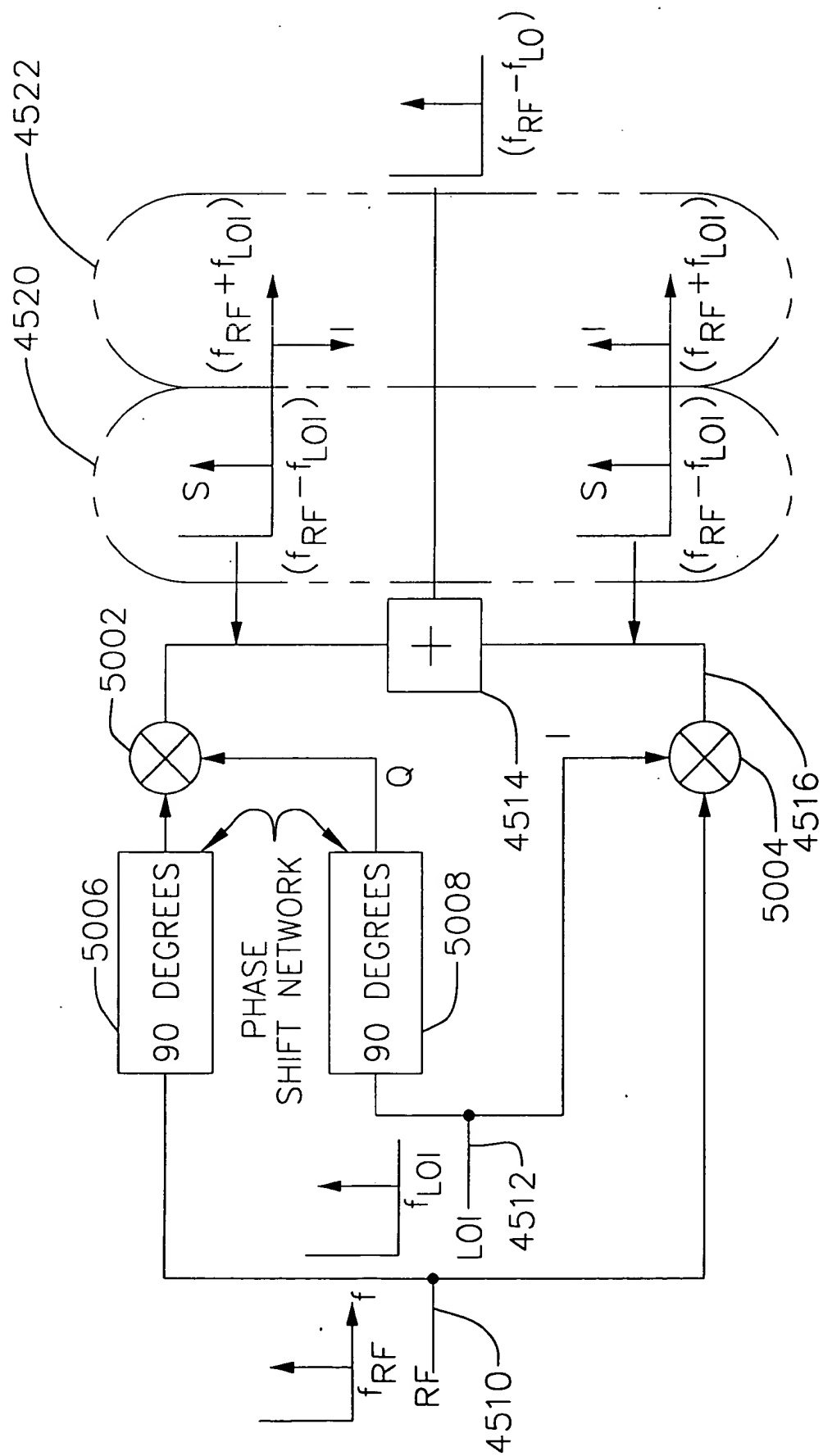


FIG. 51

EXTERNAL 36 OR 44MHz FILTER OPTION  
E.G. SIEMENS X6964 ( $f_c = 43.75\text{MHz}$ )

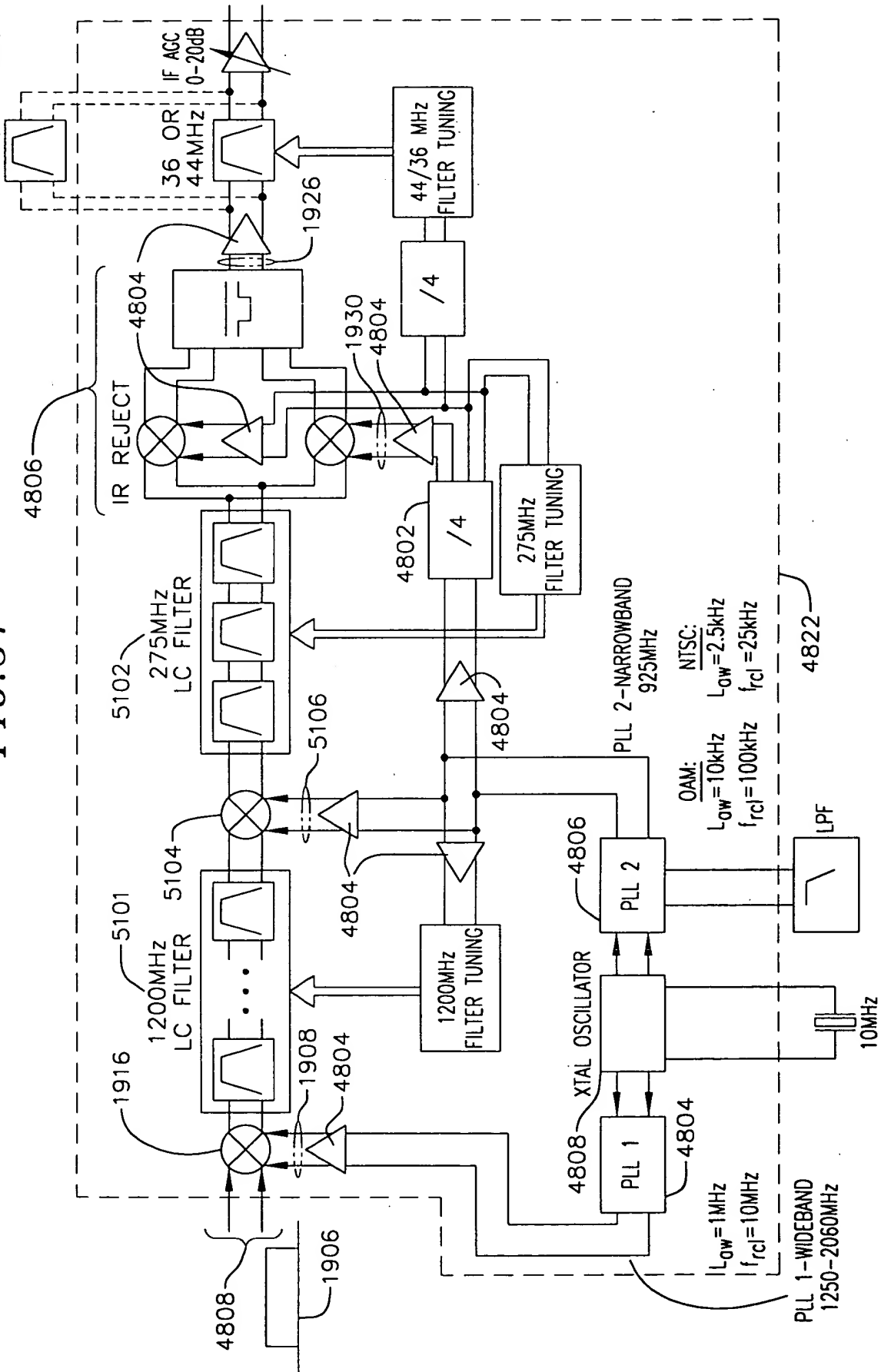
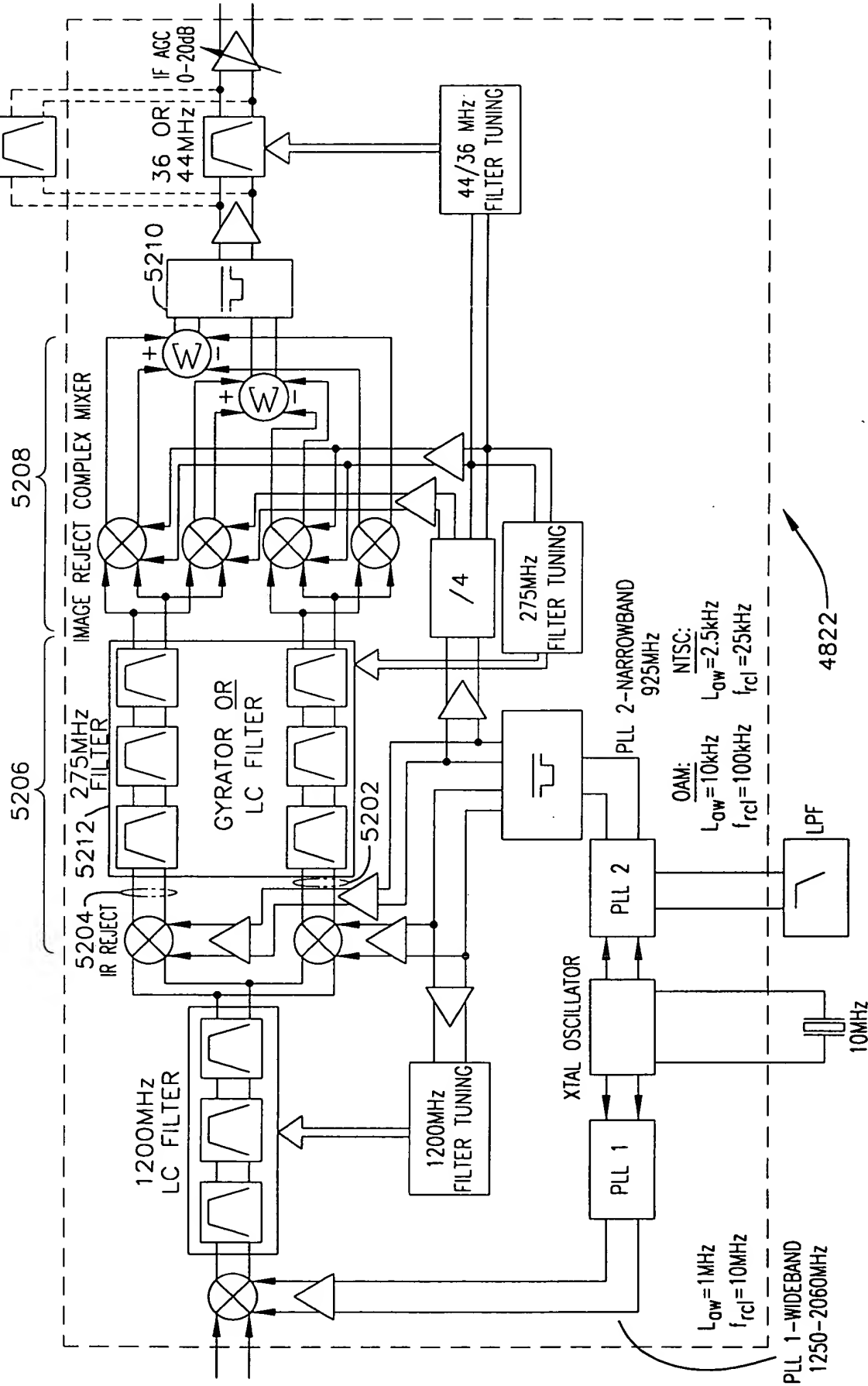


FIG. 52

EXTERNAL 36 OR 44MHz FILTER OPTION  
E.G. SIEMENS X6964 ( $f_c = 43.75\text{MHz}$ )



**FIG. 53**

CATV TUNER

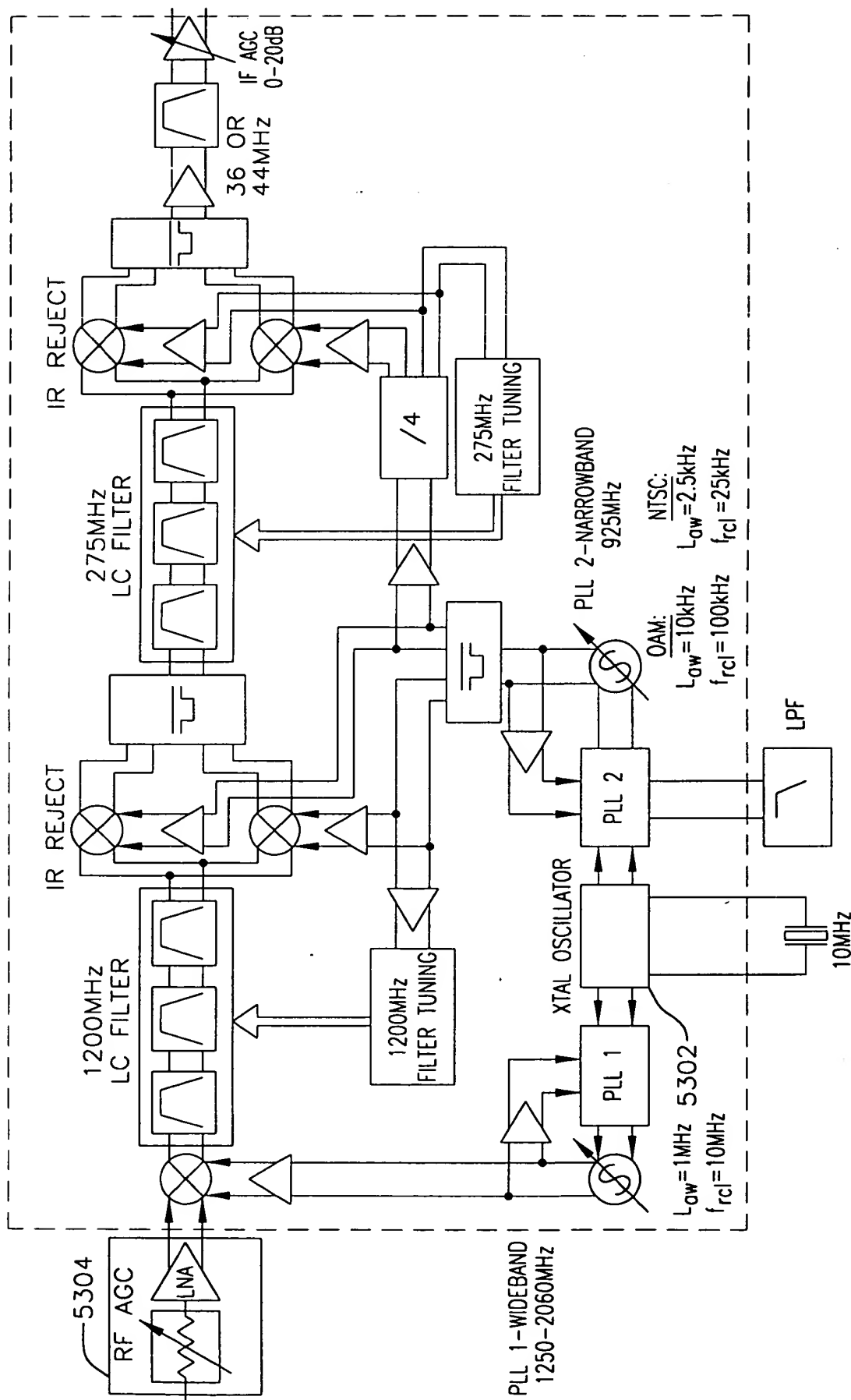
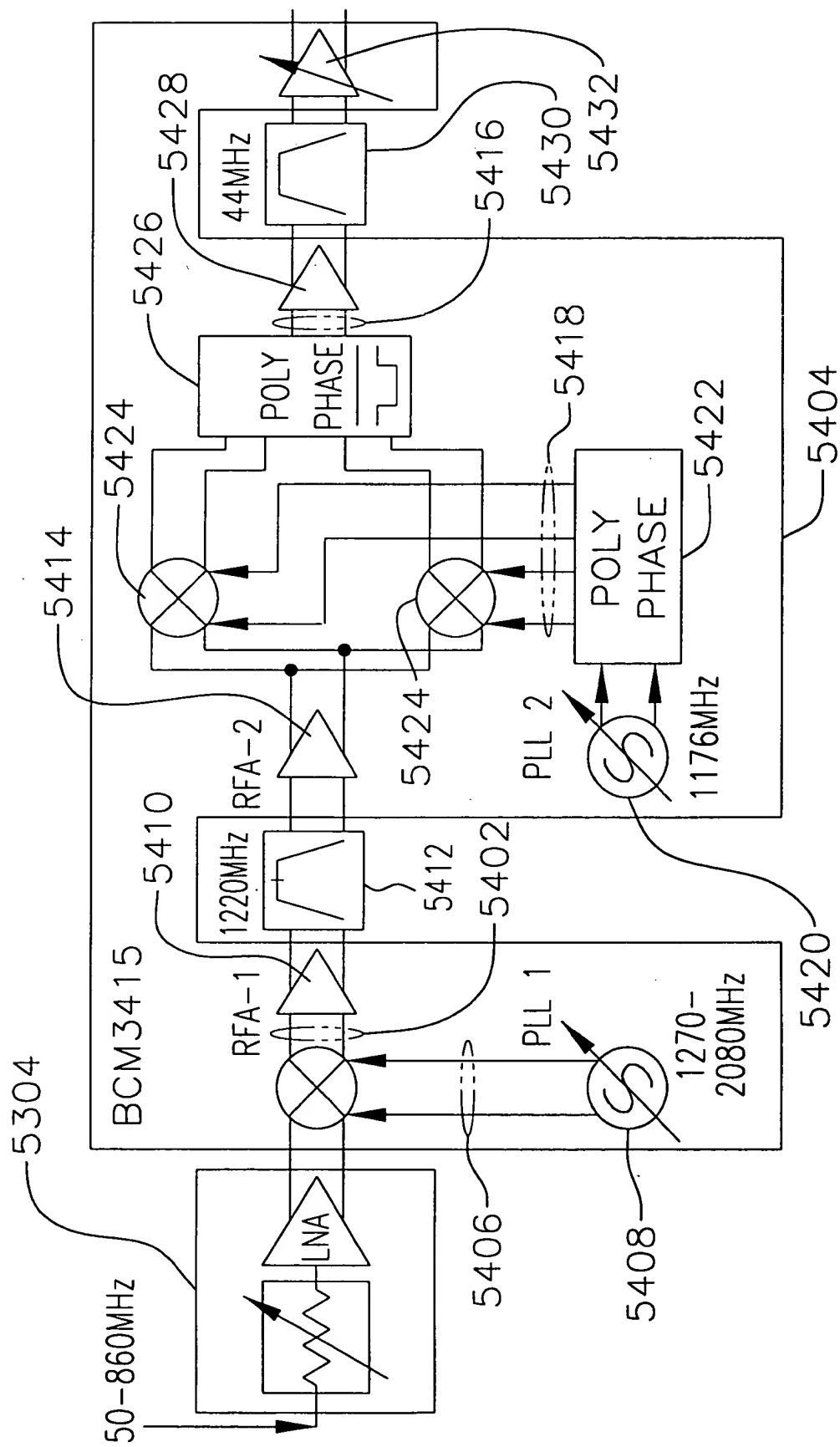
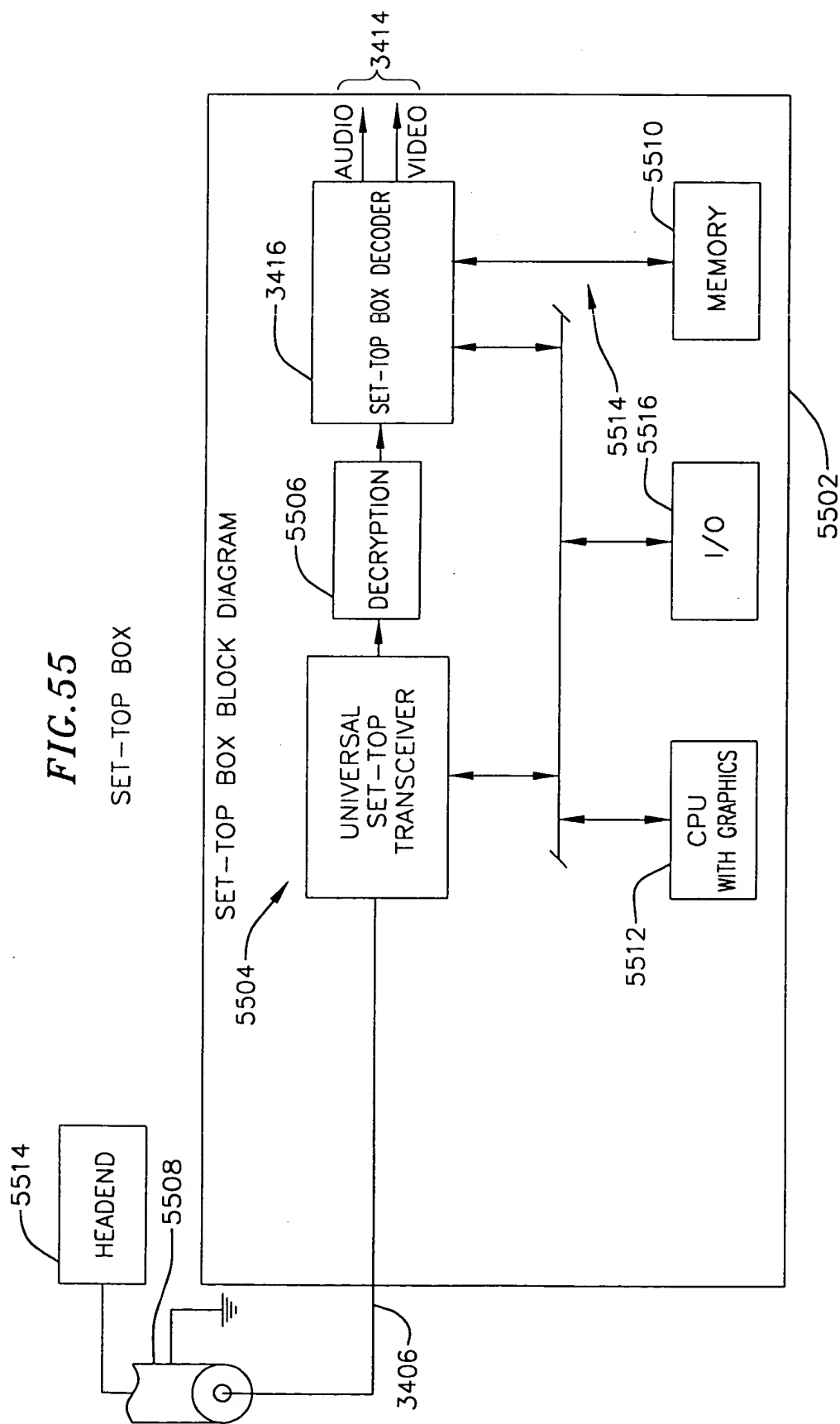
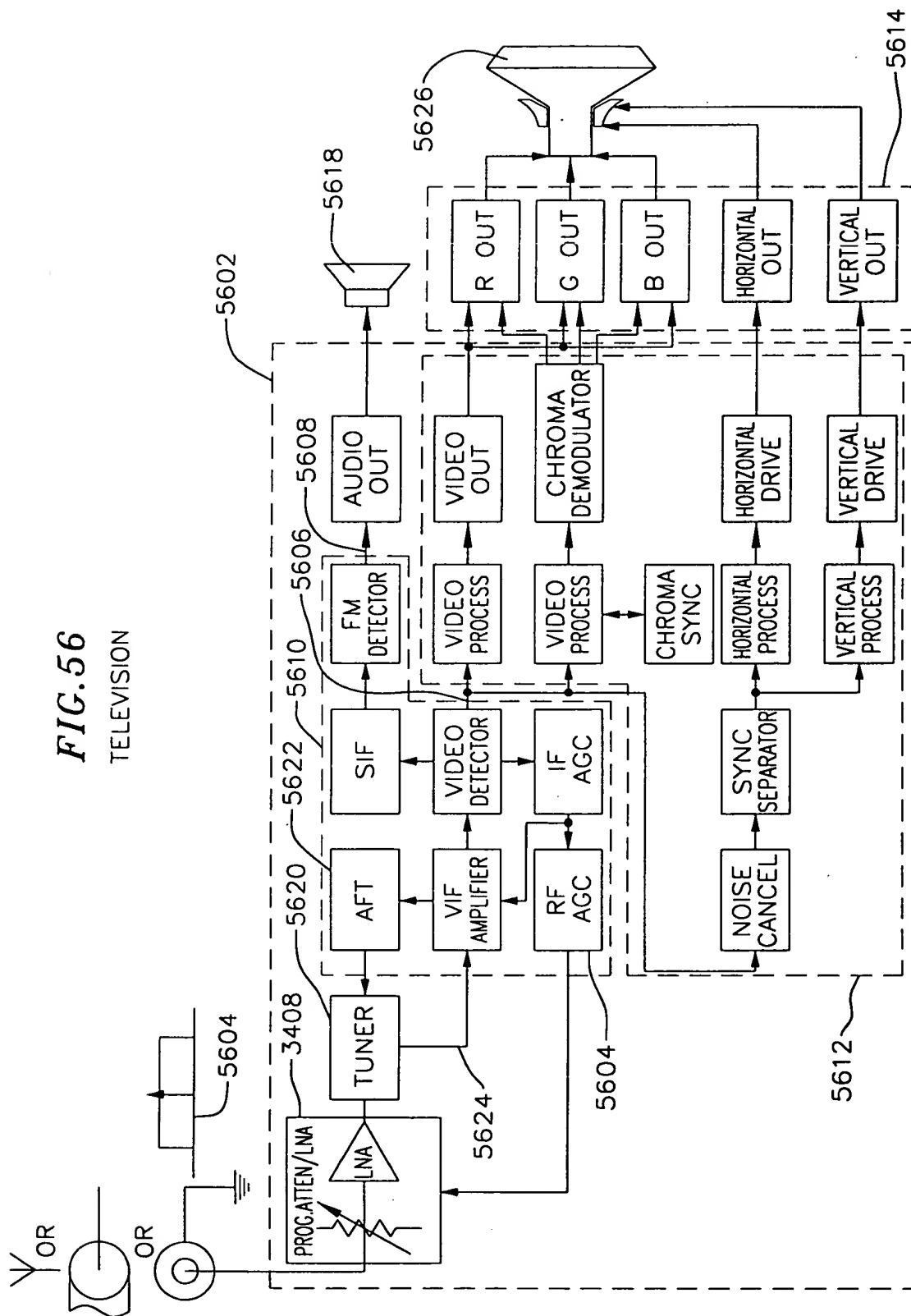


FIG. 54







**FIG.57**  
VCR BLOCK DIAGRAM

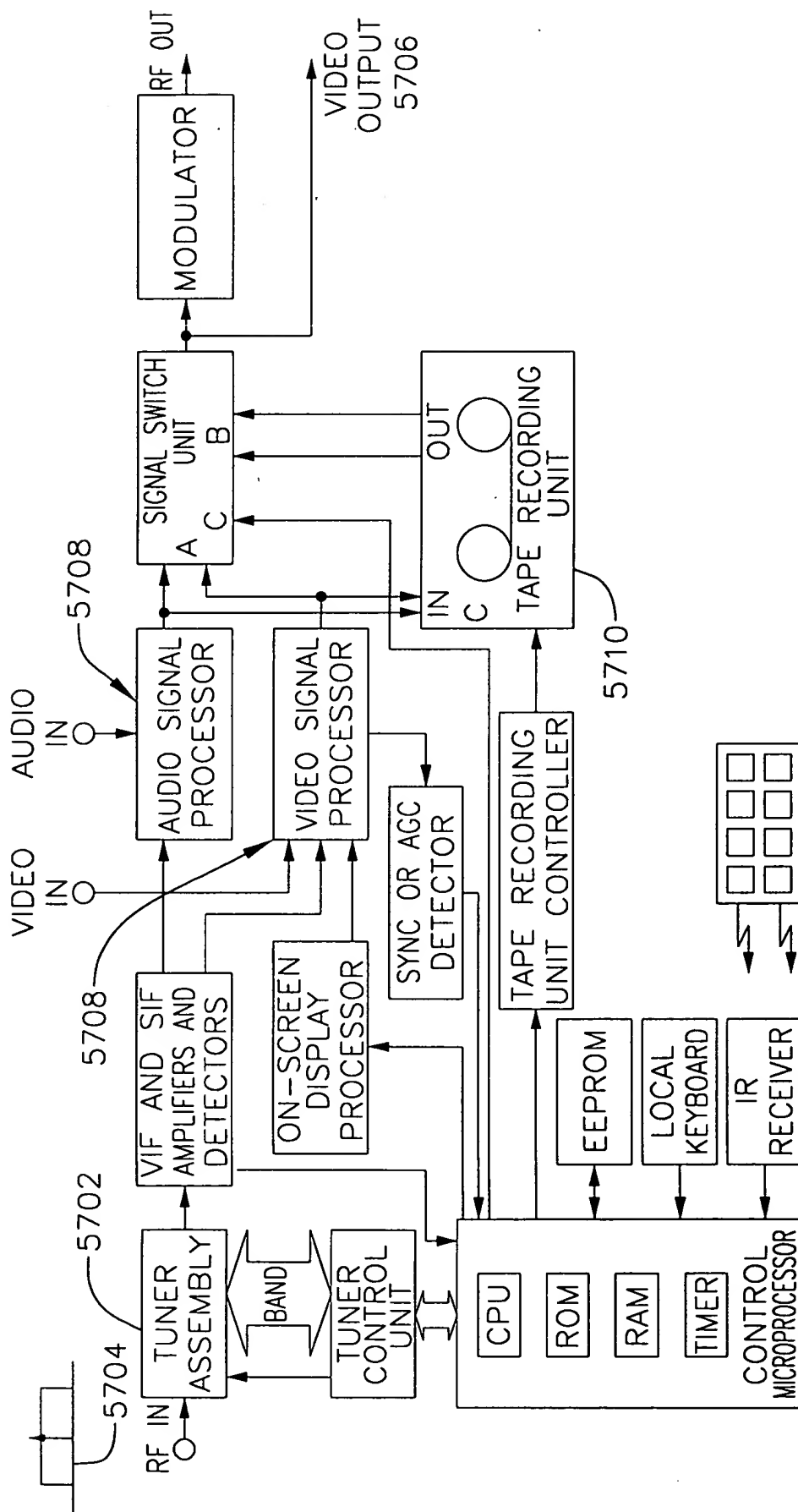




FIG. 58

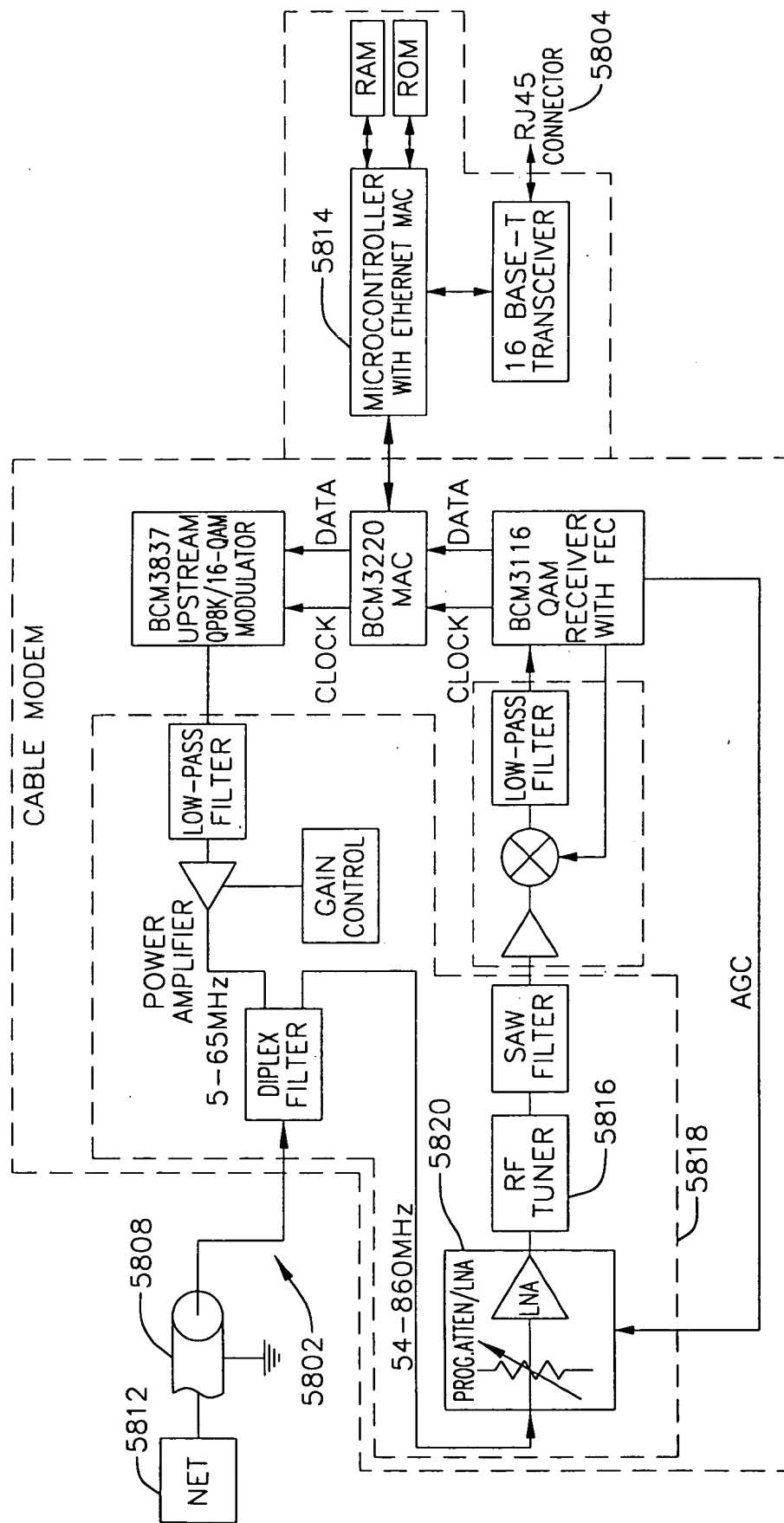




FIG.59

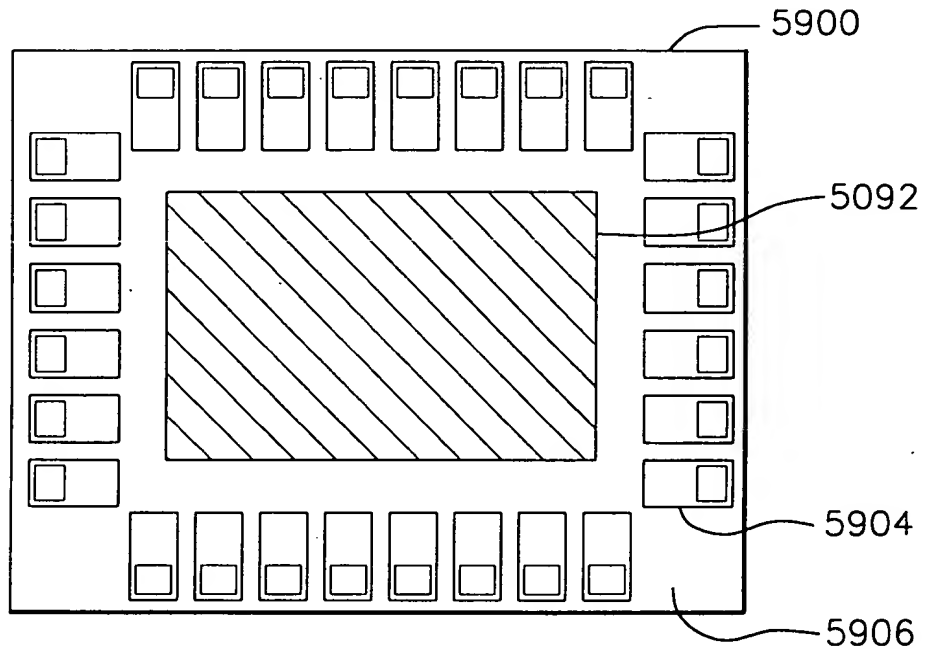


FIG.60

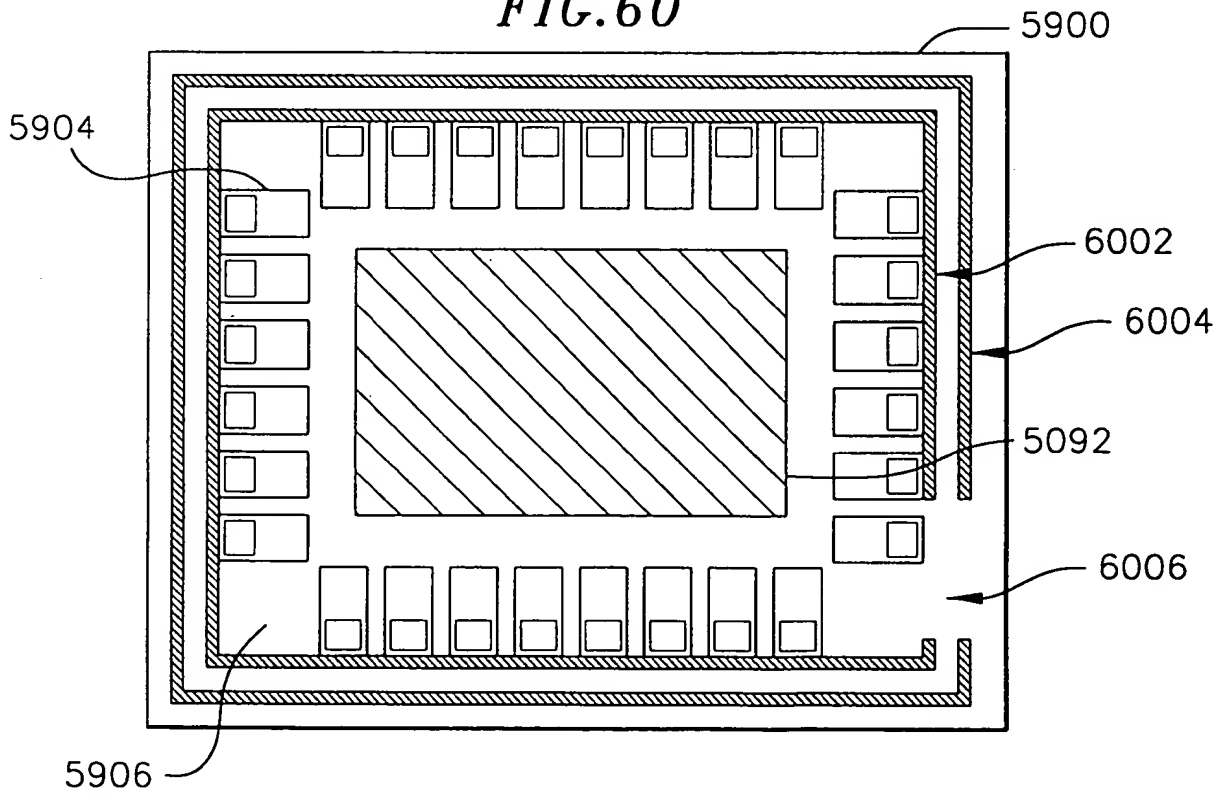


FIG. 61

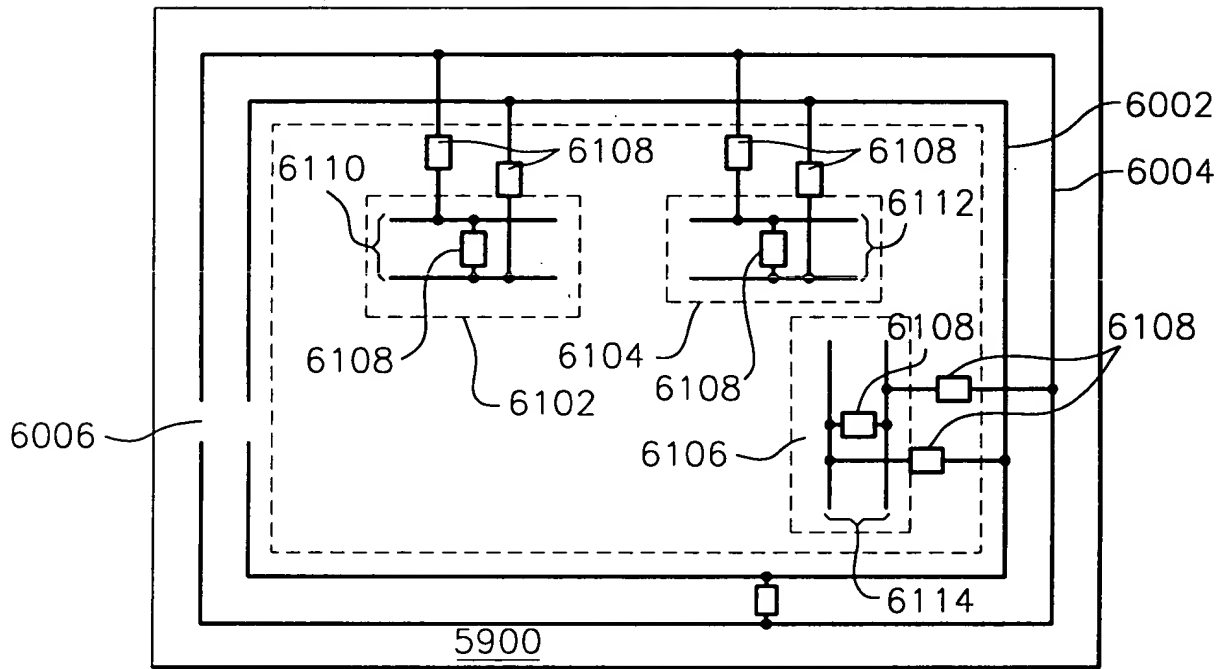
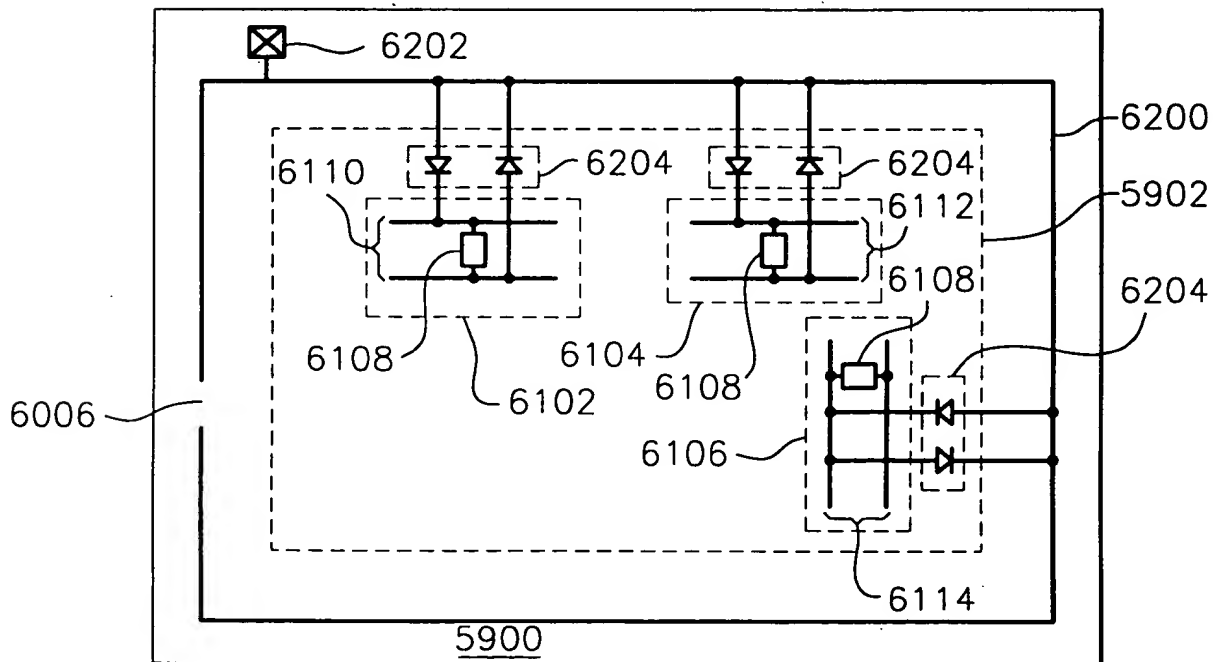
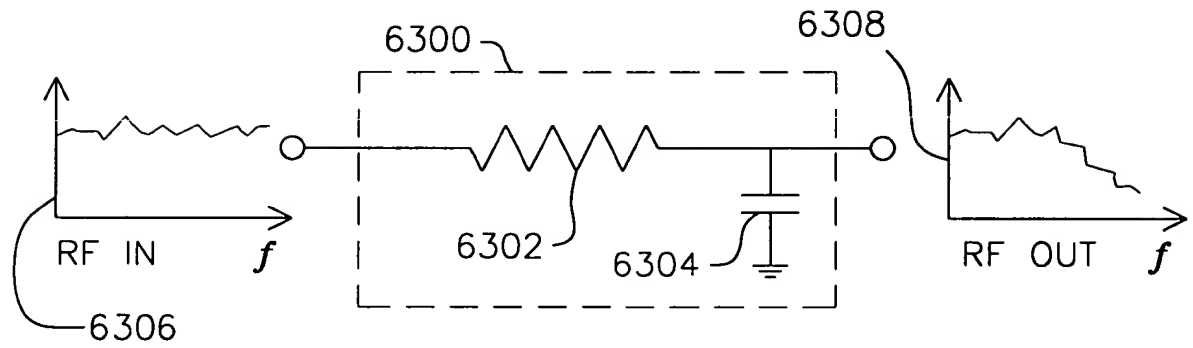


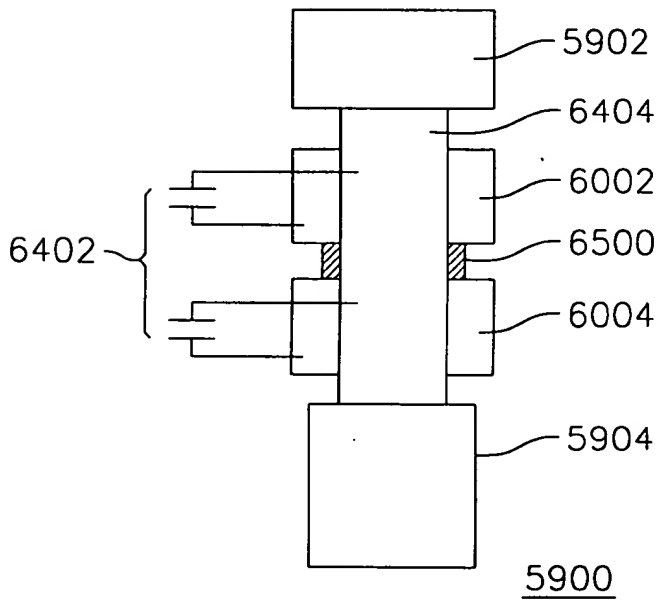
FIG. 62



*FIG. 63*



*FIG. 64*



*FIG. 65*

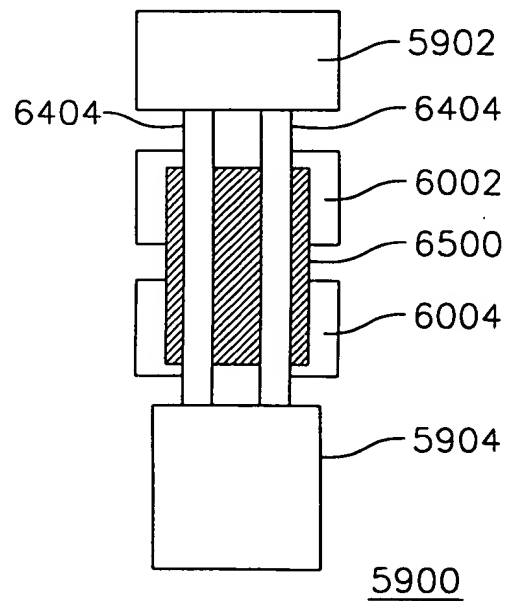


FIG. 66

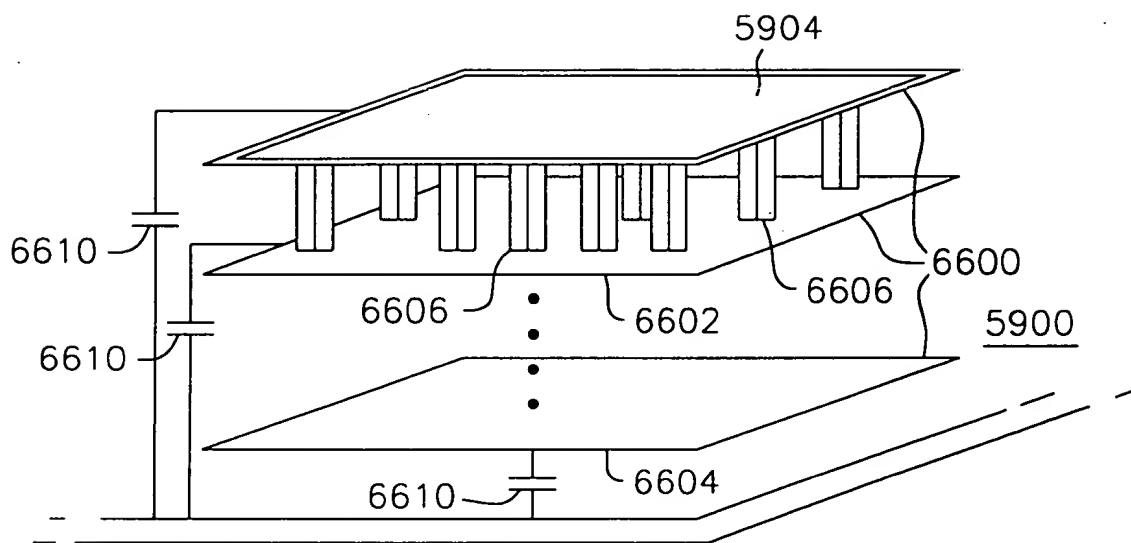


FIG. 67

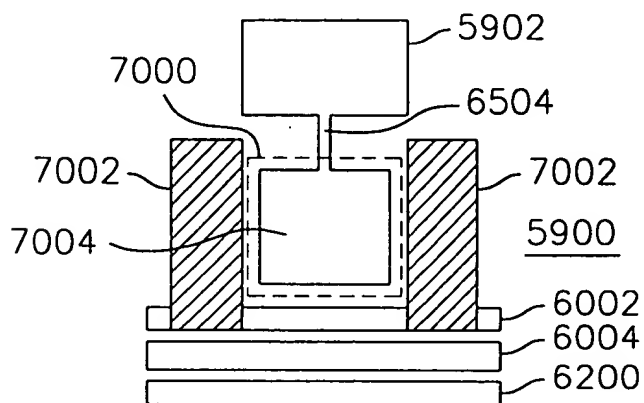
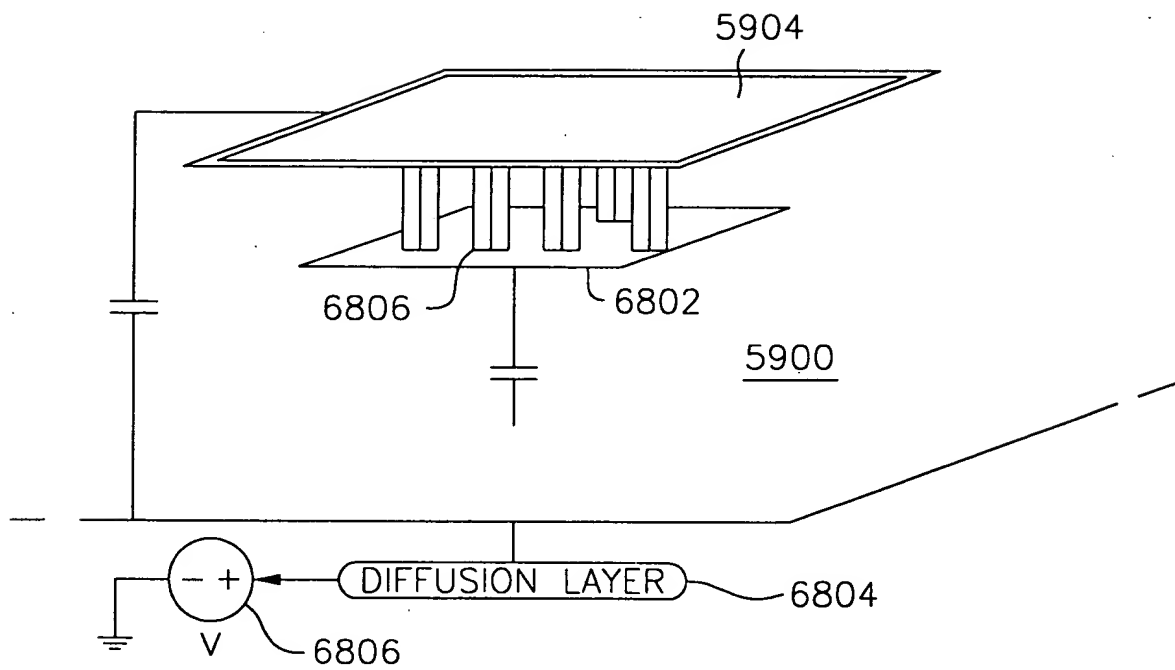
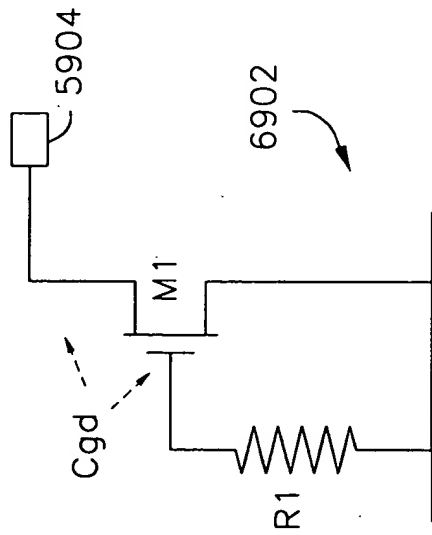


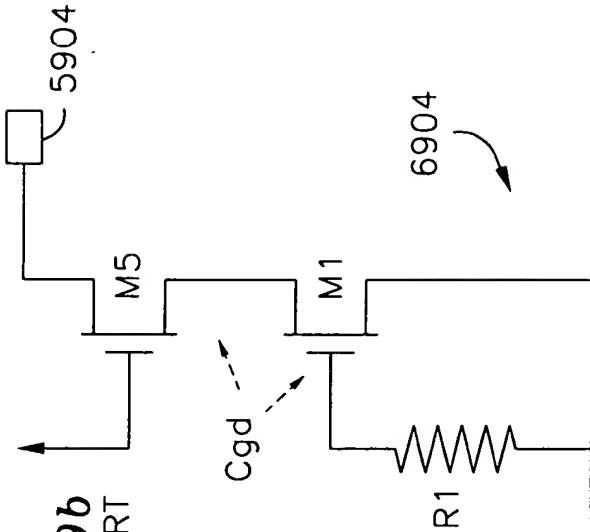
FIG. 68



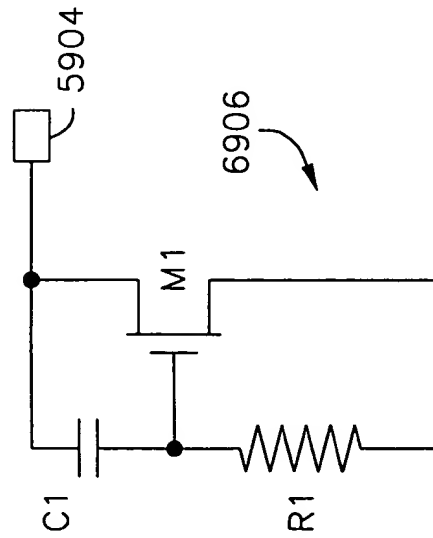
**FIG. 69a**  
PRIOR ART



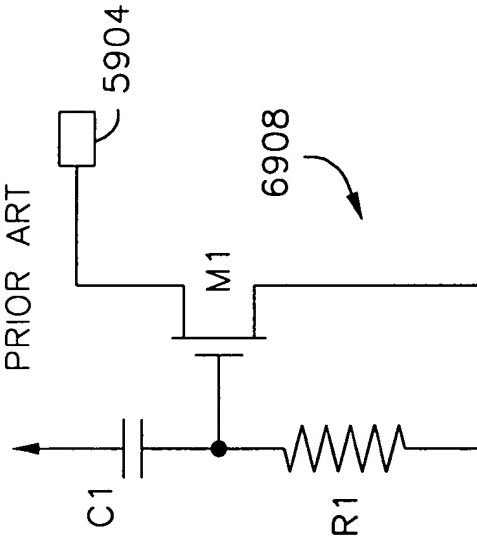
**FIG. 69b**  
PRIOR ART



**FIG. 69c**  
PRIOR ART



**FIG. 69d**  
PRIOR ART



**FIG. 69e**  
PRIOR ART

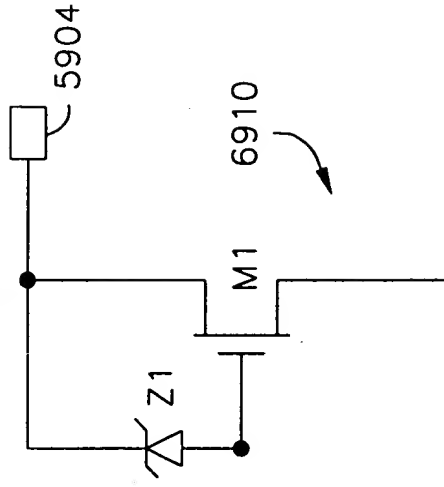


FIG. 70

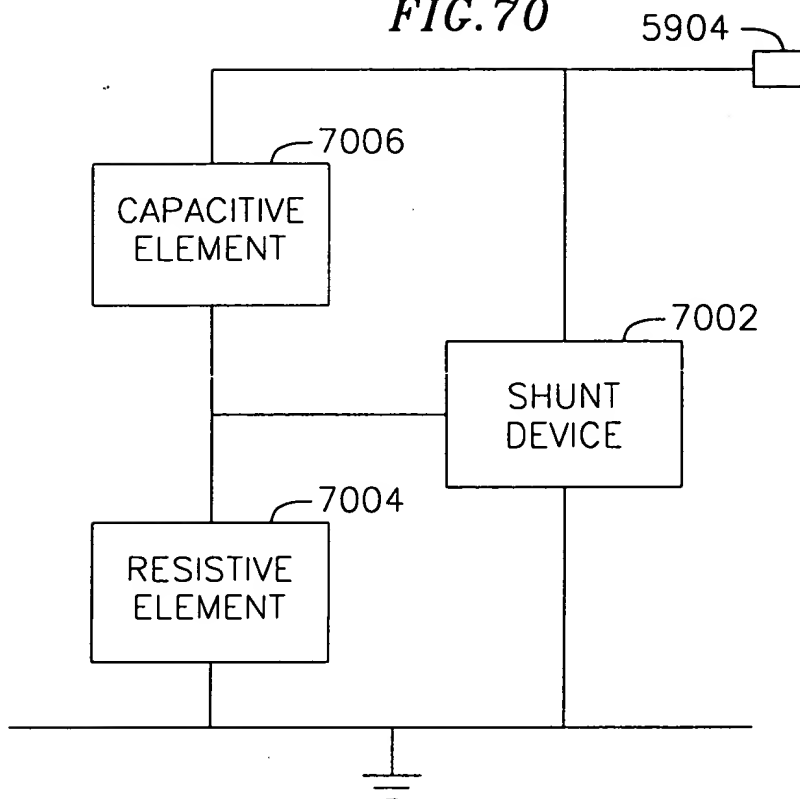


FIG. 71

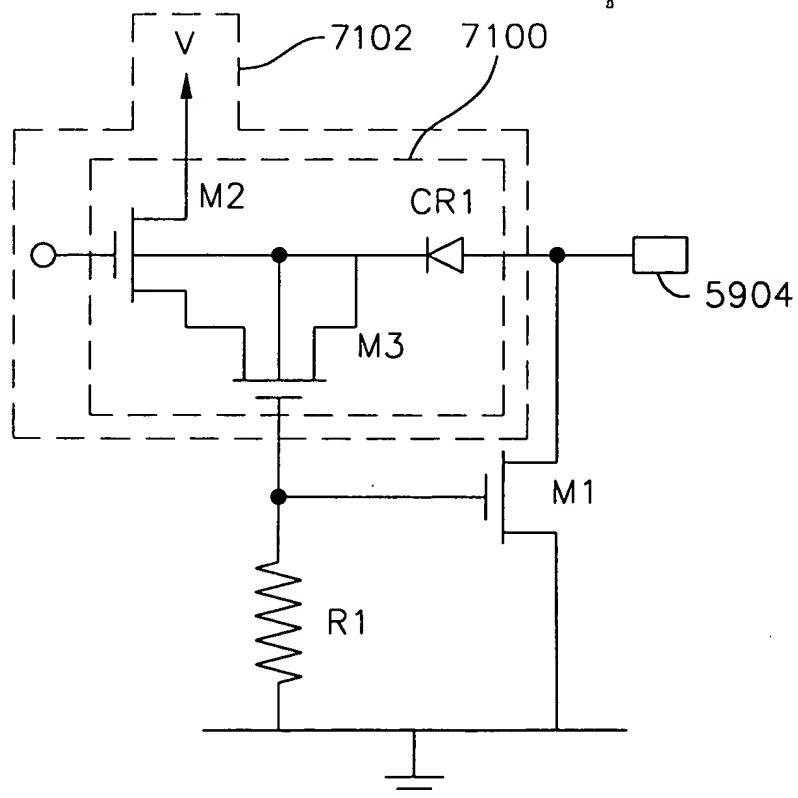




FIG. 72

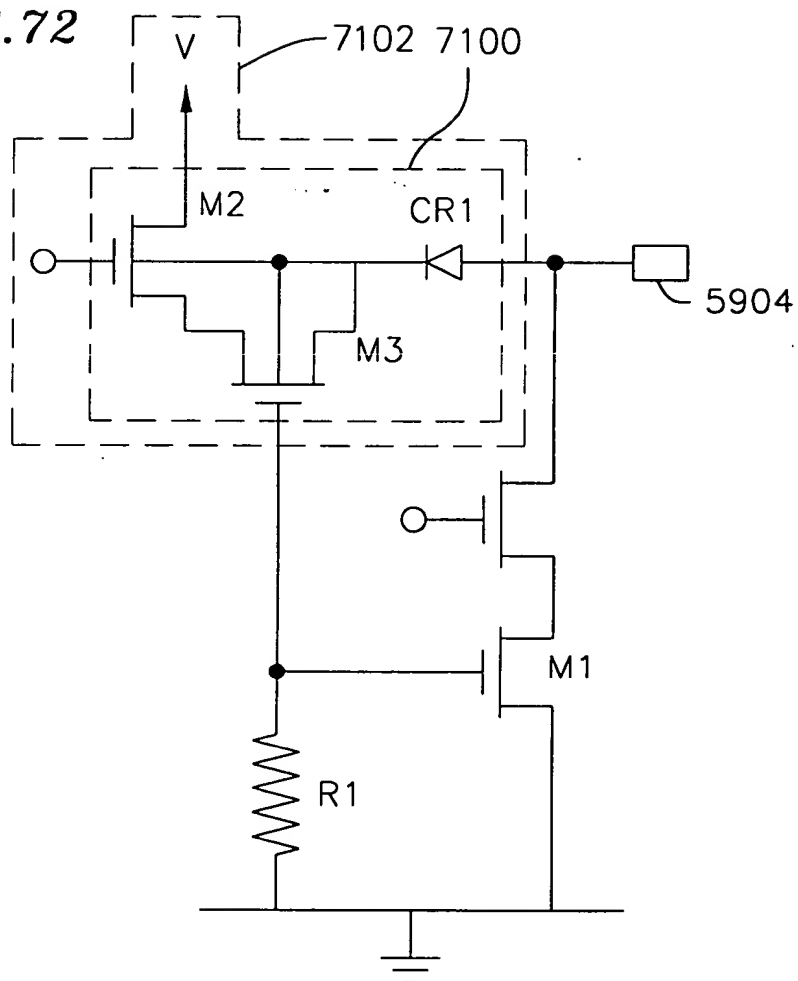


FIG. 73

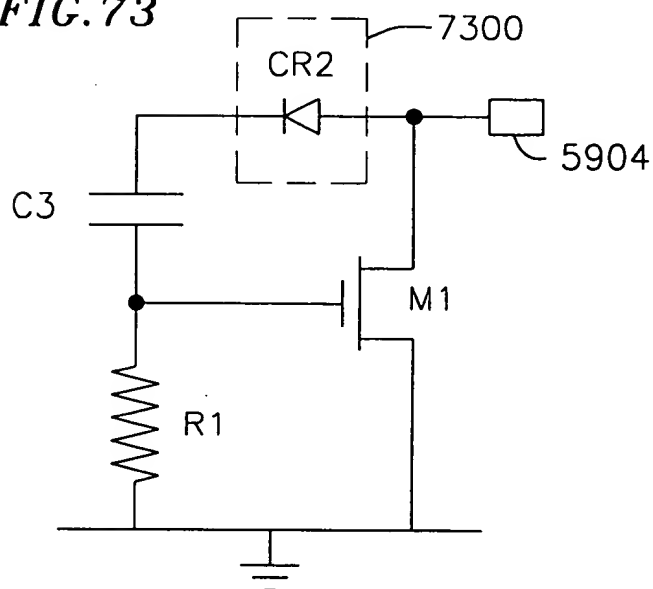


FIG. 74

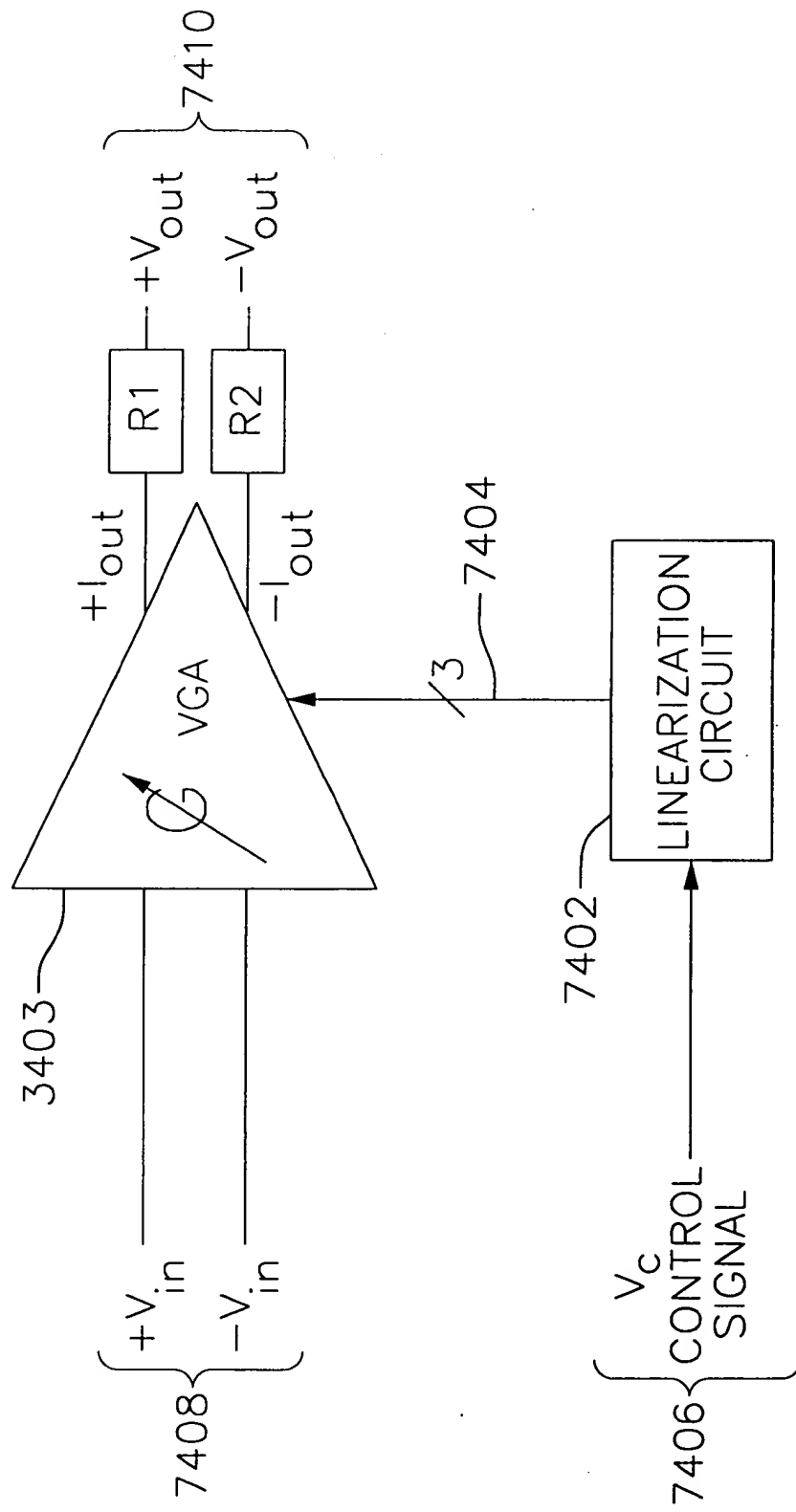
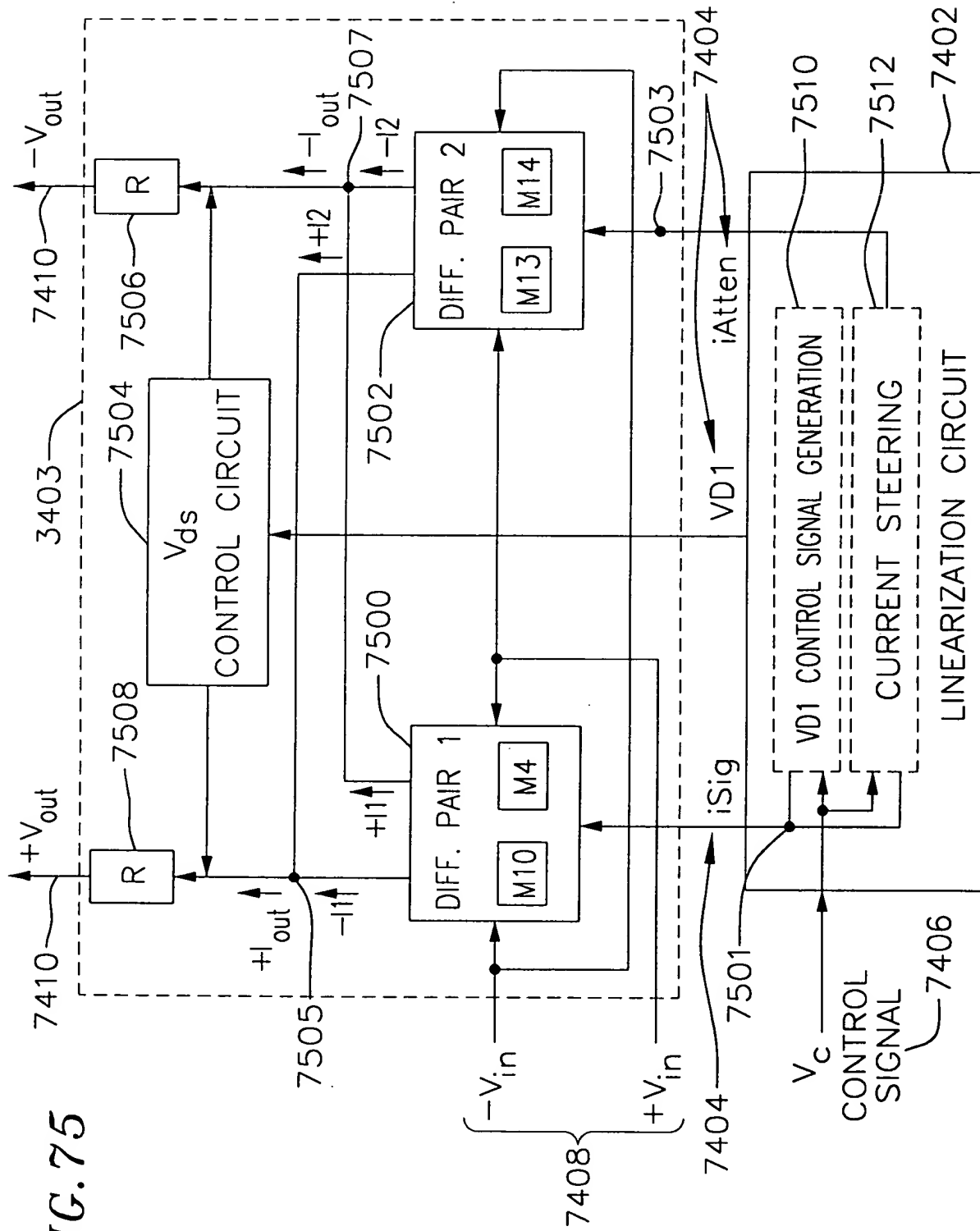


FIG. 75



*FIG. 76*

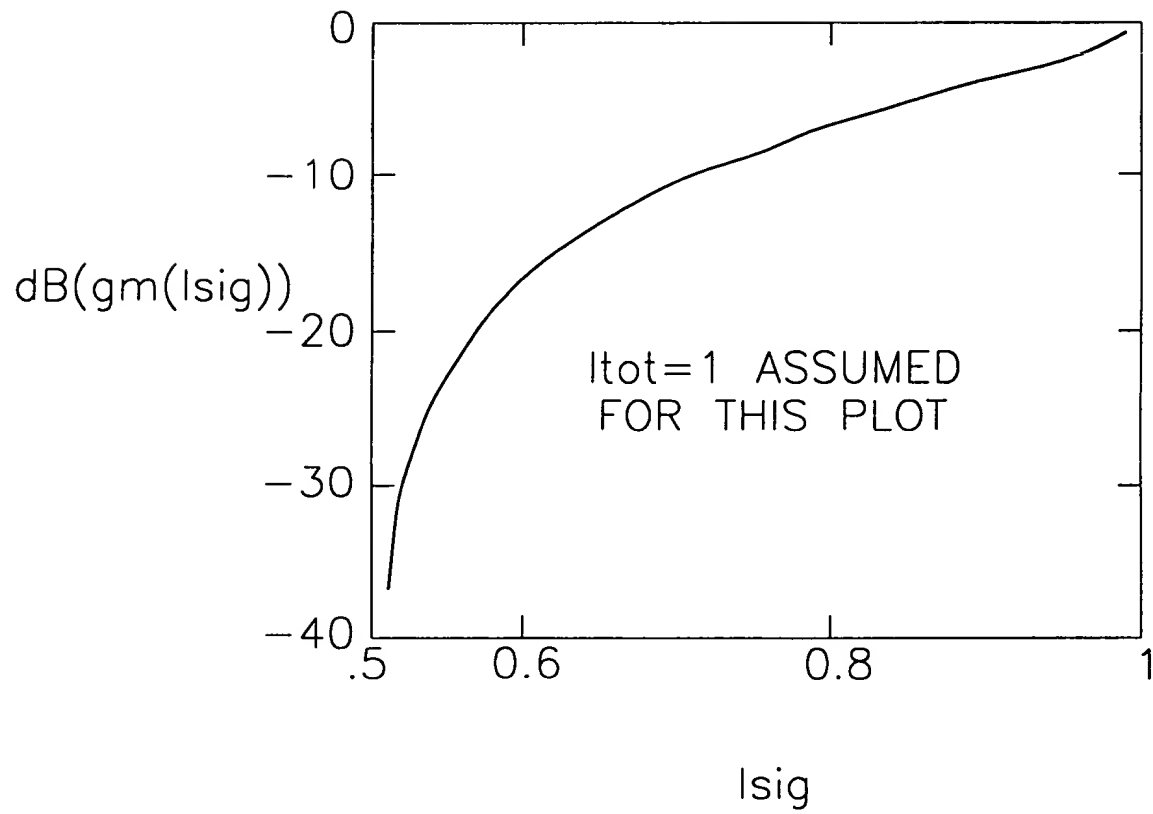


FIG. 77

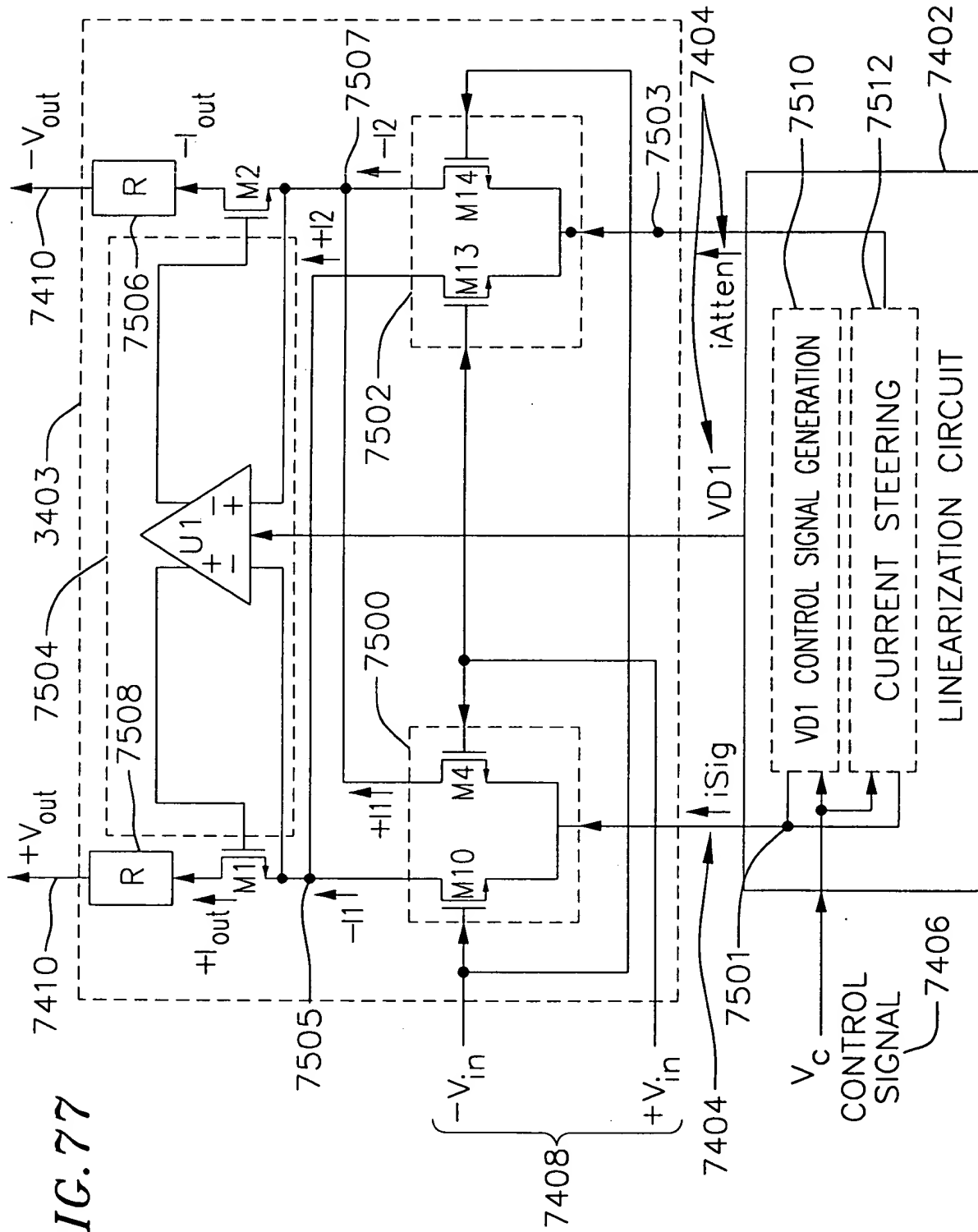


FIG. 78a

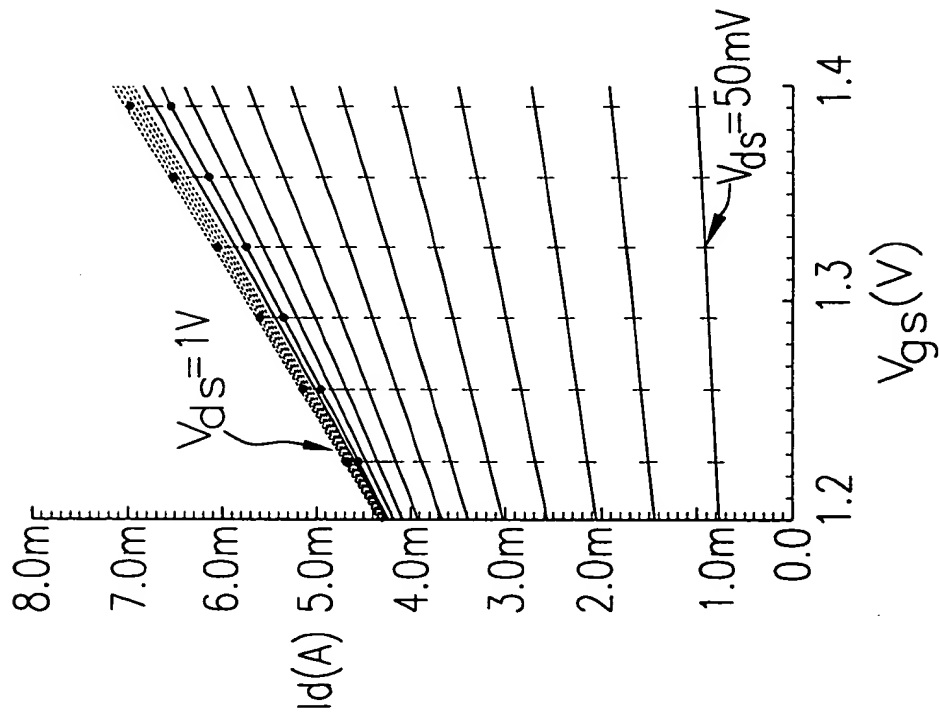


FIG. 78b

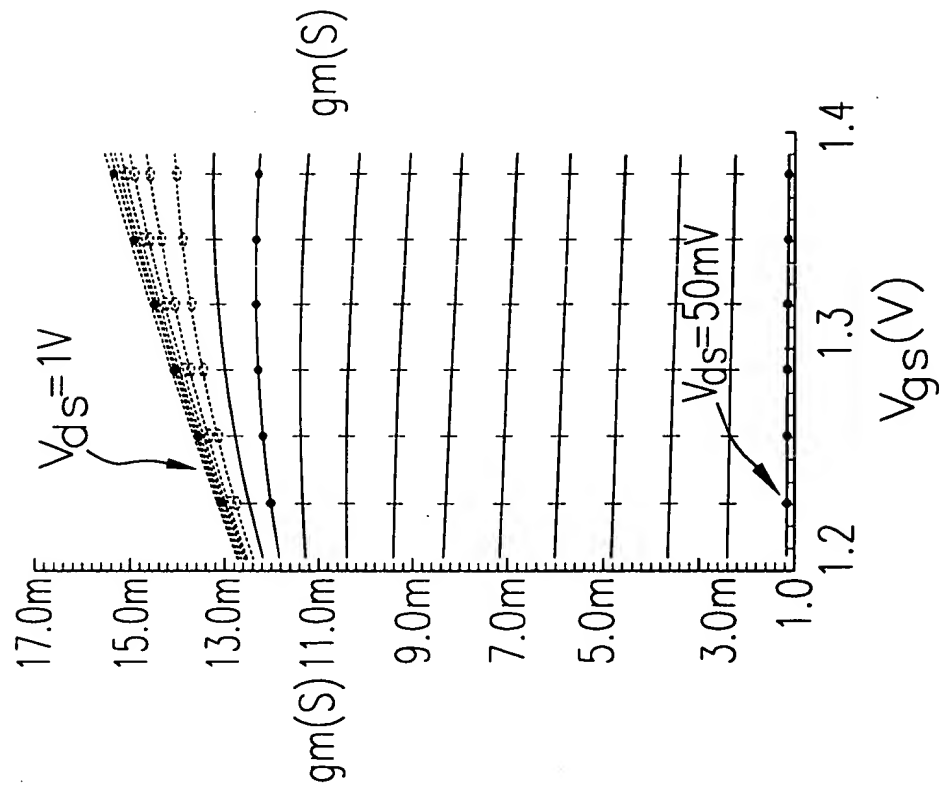


FIG. 78c

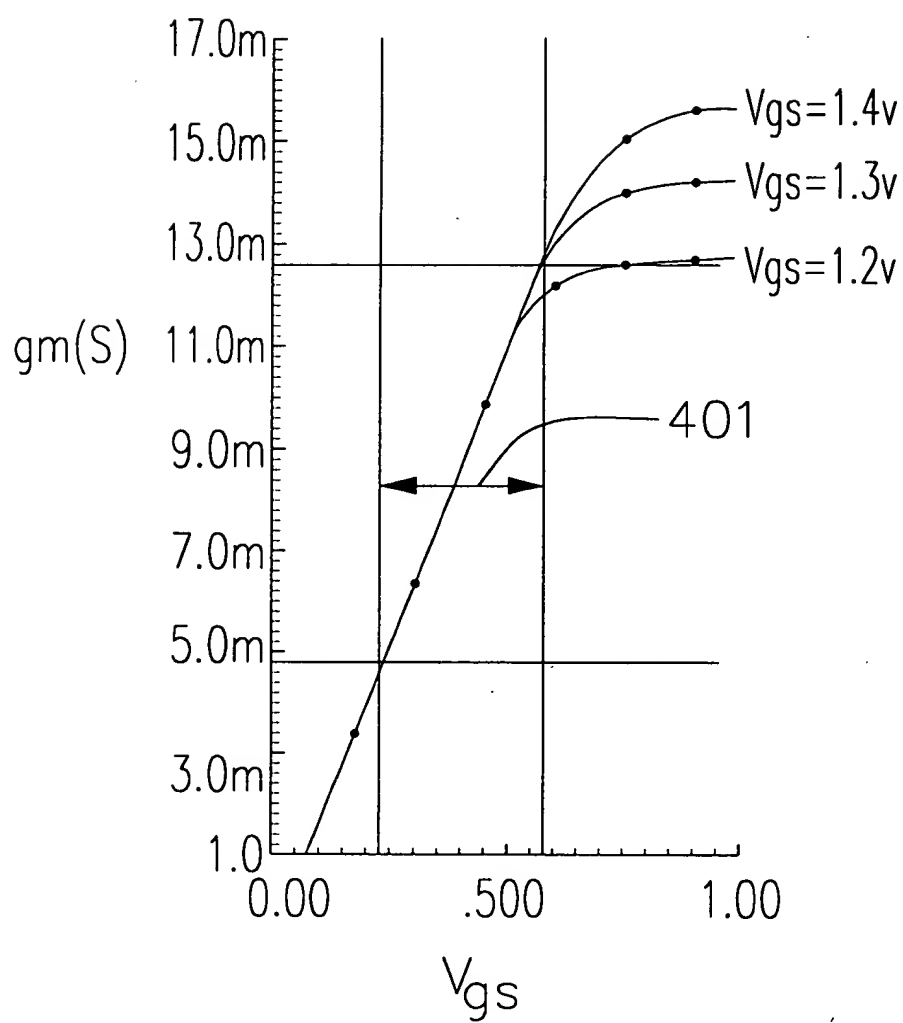


FIG. 79

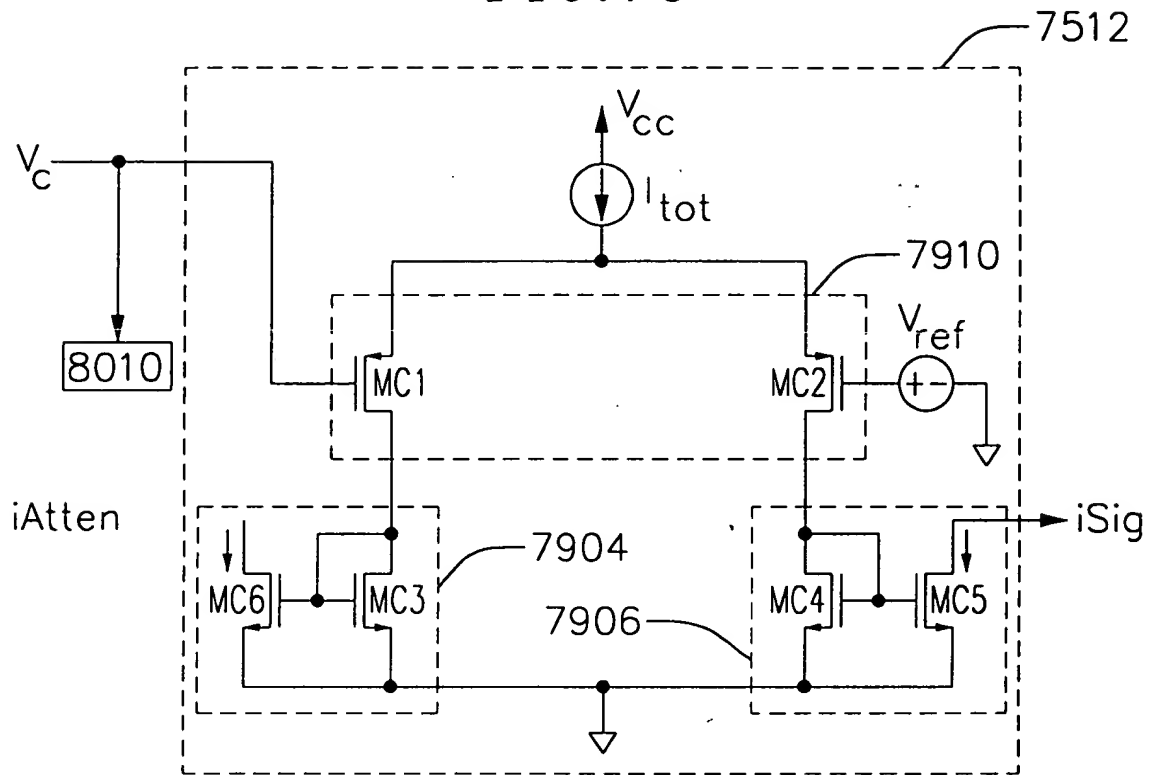
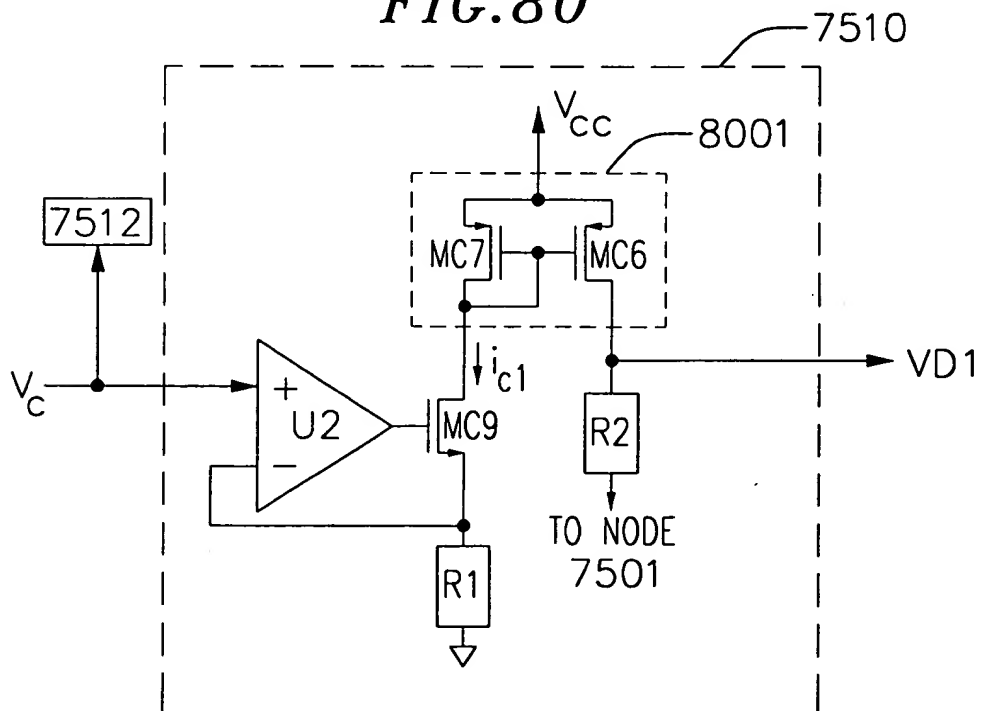
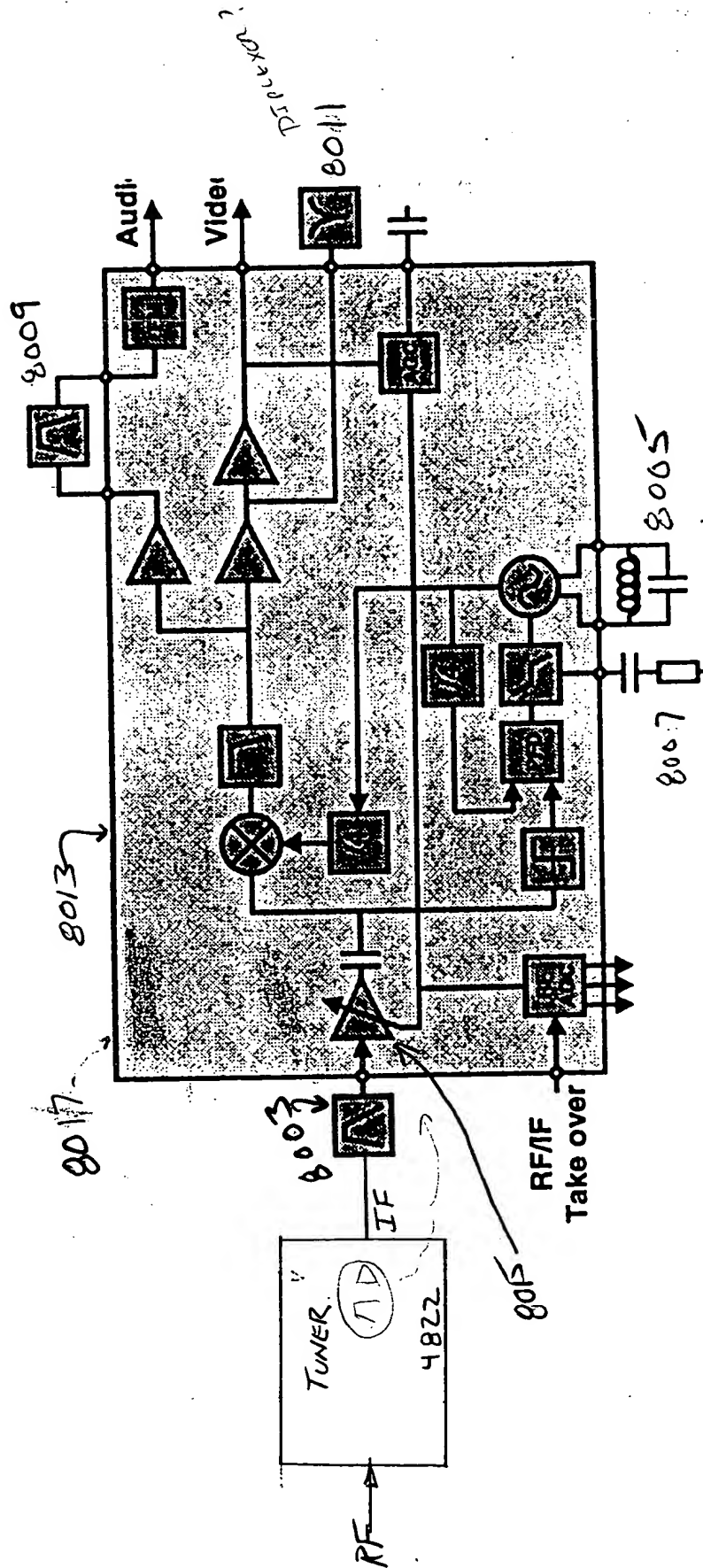


FIG. 80







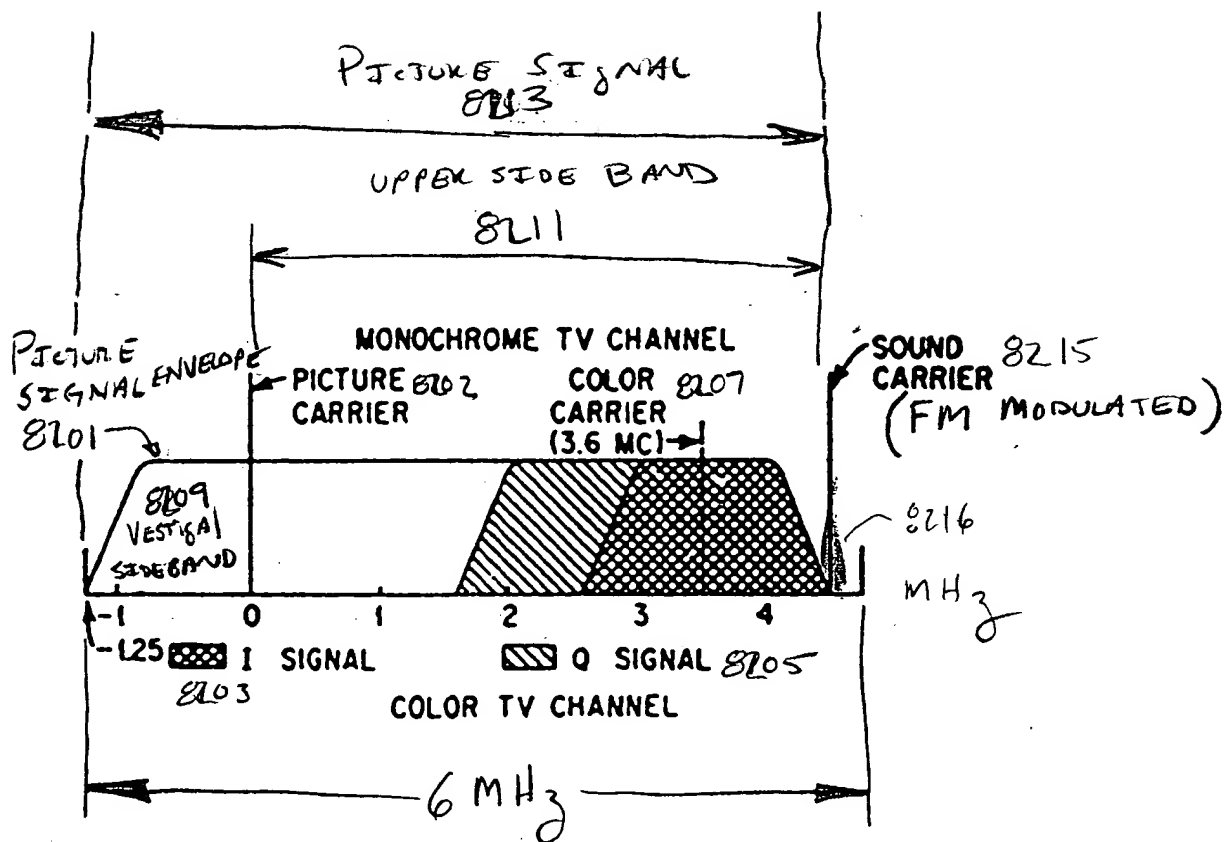


FIG. 82

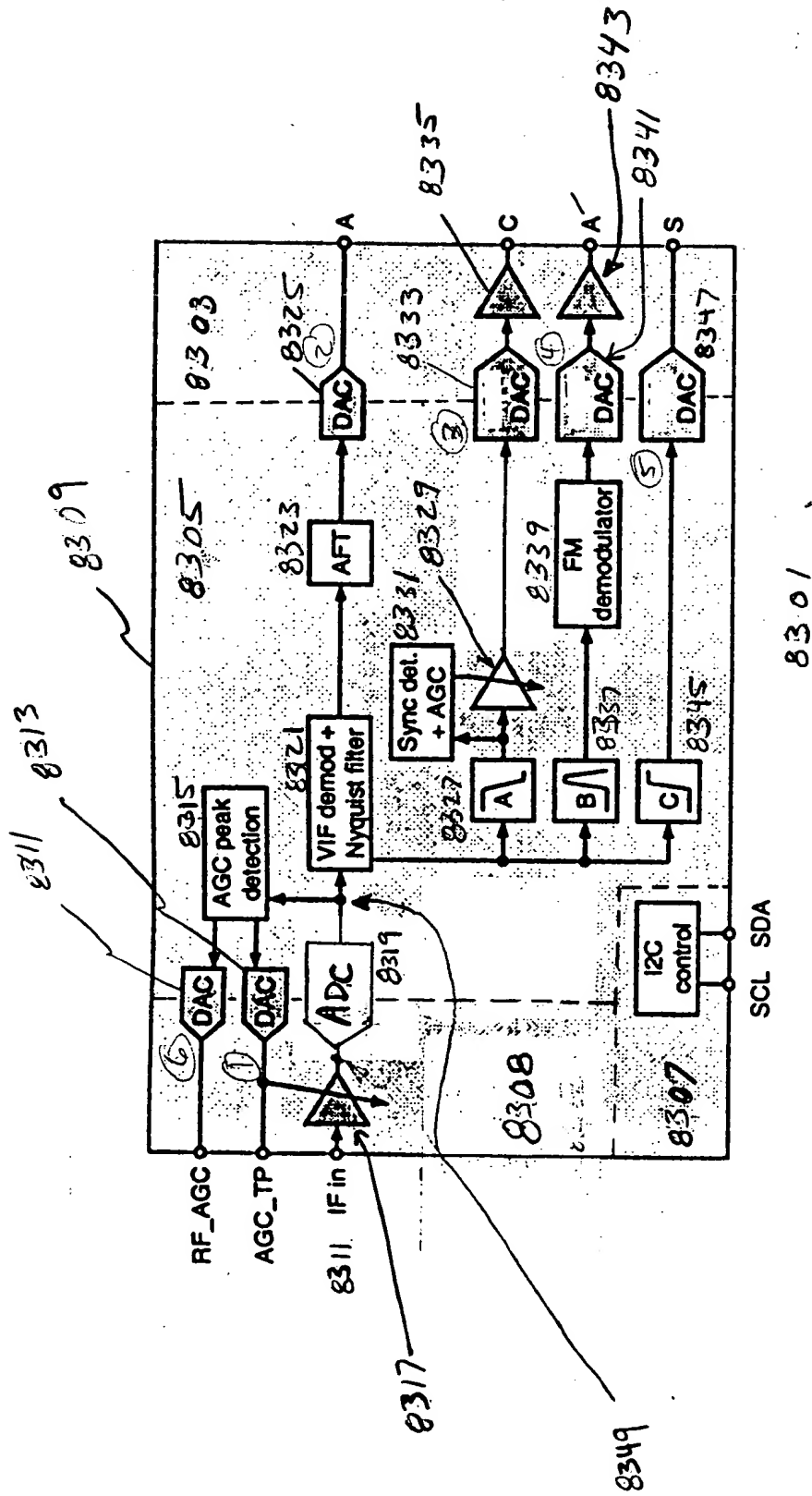


FIG. 83

FIG. 84a

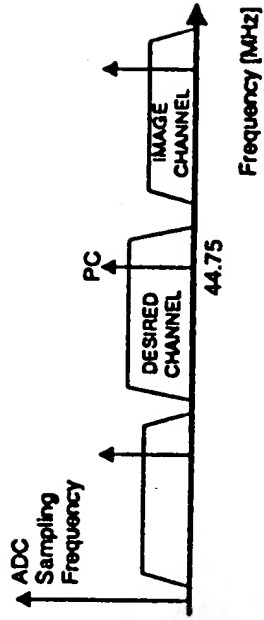


FIG. 84b

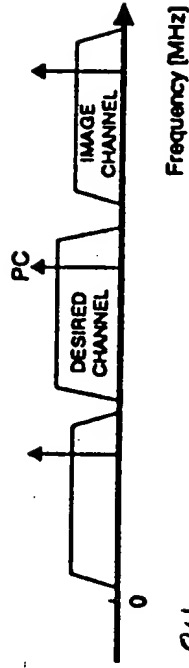


FIG. 84c

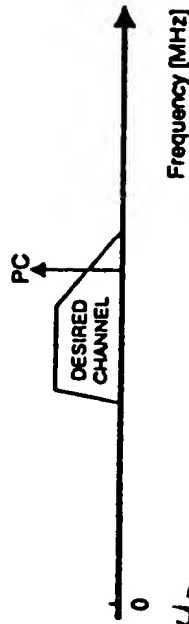
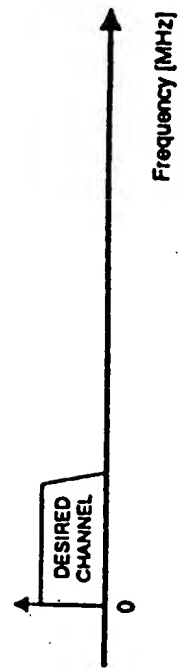


FIG. 84d



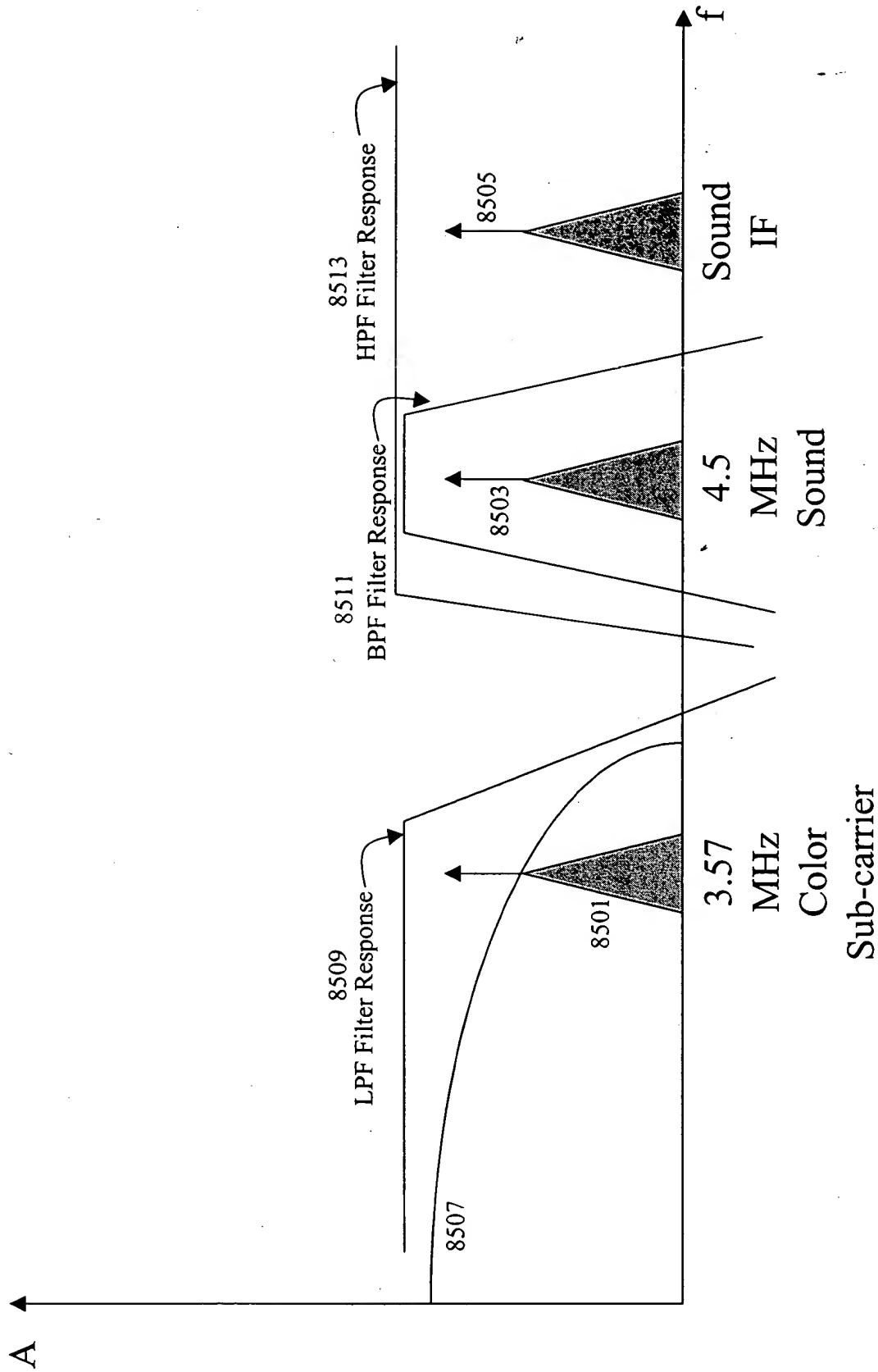


FIG. 85